Sigma-Delta
New algorithms and Techniques

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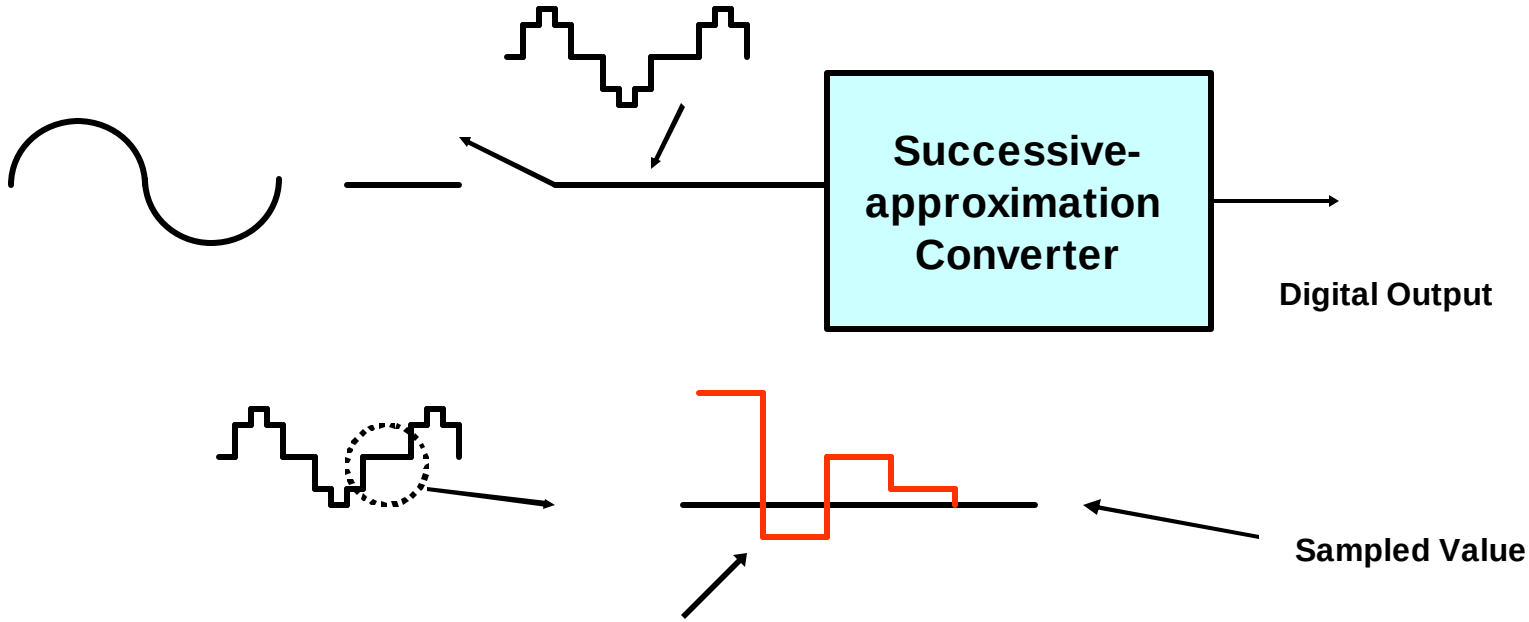
ANALOG DEVICES

Outline

- Intro: SAR vs Sigma-Delta
- New conversion architectures driven from practical needs in the integrated circuit industry
  - From 1-bit to Multi-bit
  - Multi-bit Mismatch Shaping
  - Split Noise-shaping – noise-shaped segmentation
  - Continuous-time (CT) DACs
  - Mixed CT/DT (continuous/discrete) ADCs
- Power Sigma-Delta (“class-D” amplifiers)
  - Using dynamic hysteresis to reduce the output transition rate
- Research work
  - Multiplying Two 1-bit signals and getting a noise-shaped result
  - Single-structure sigma-delta/successive-approximation; a converging time-domain view of sigma-delta
  - Noise-shaping and Prime Numbers

The Two Competing Views ...

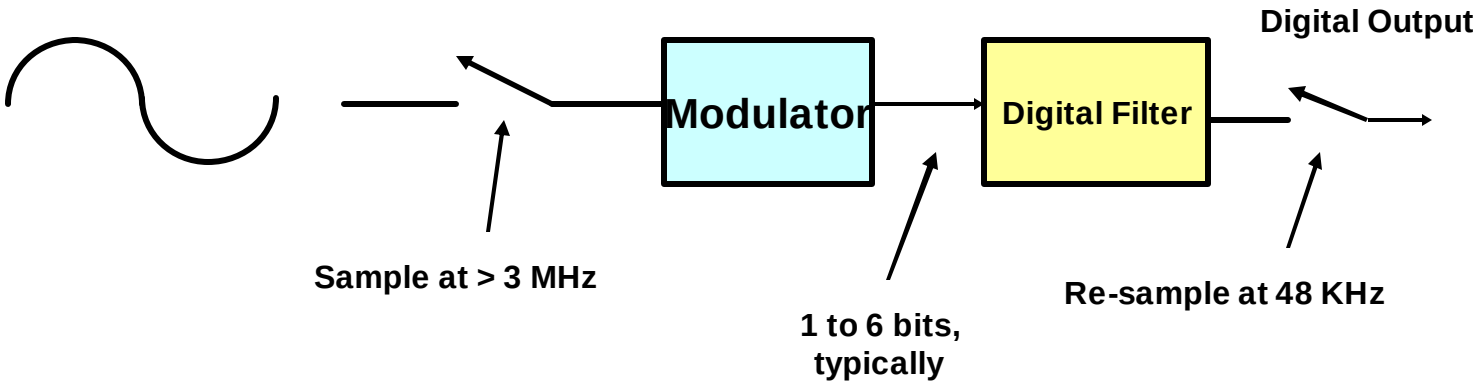
Take a sample, convert the sample with as much accuracy as possible.



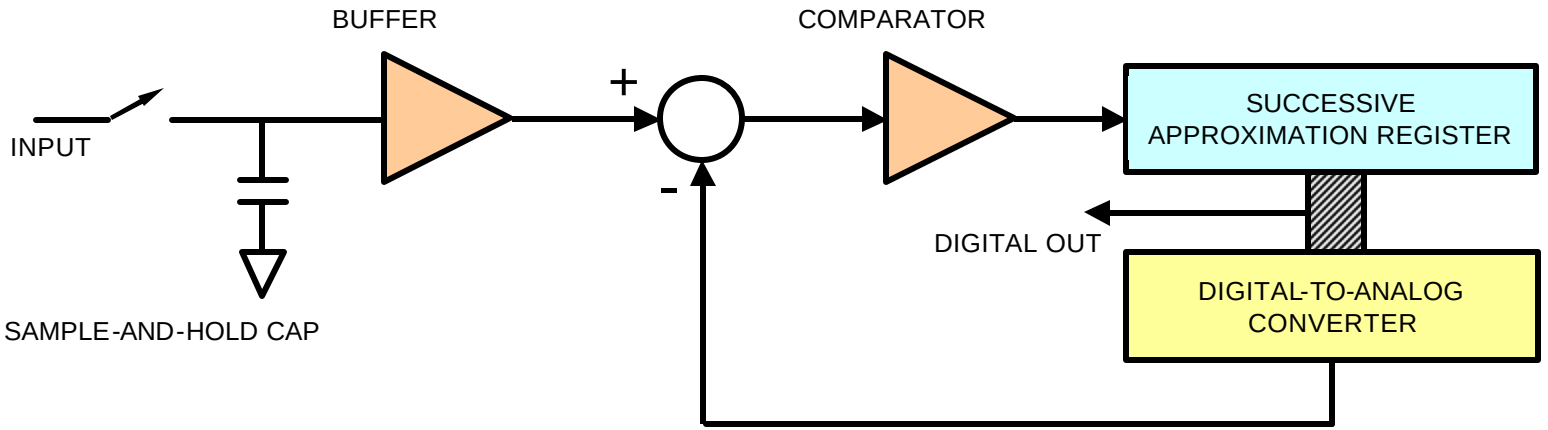
SAR algorithm is "zeroing in" on the value, cutting the search range by 2 every iteration.

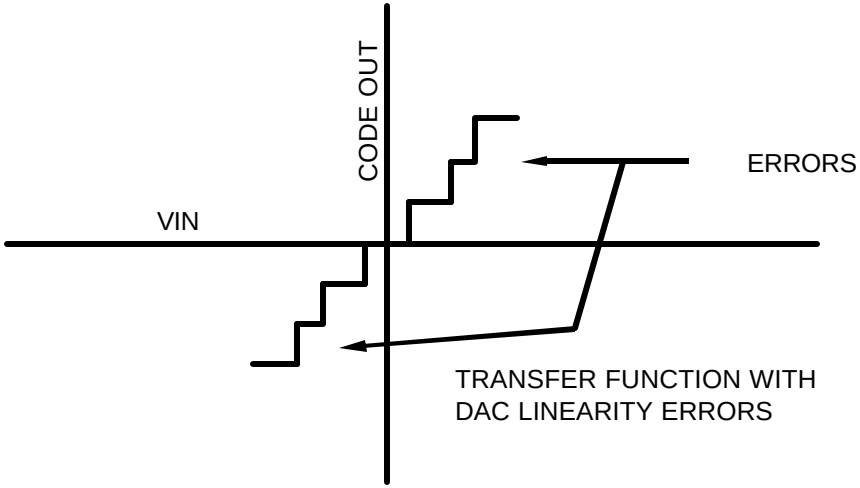
The Two Competing Views ...

Oversample at > 3MHz, apply to a "Modulator", filter the low-resolution output to recover the signal

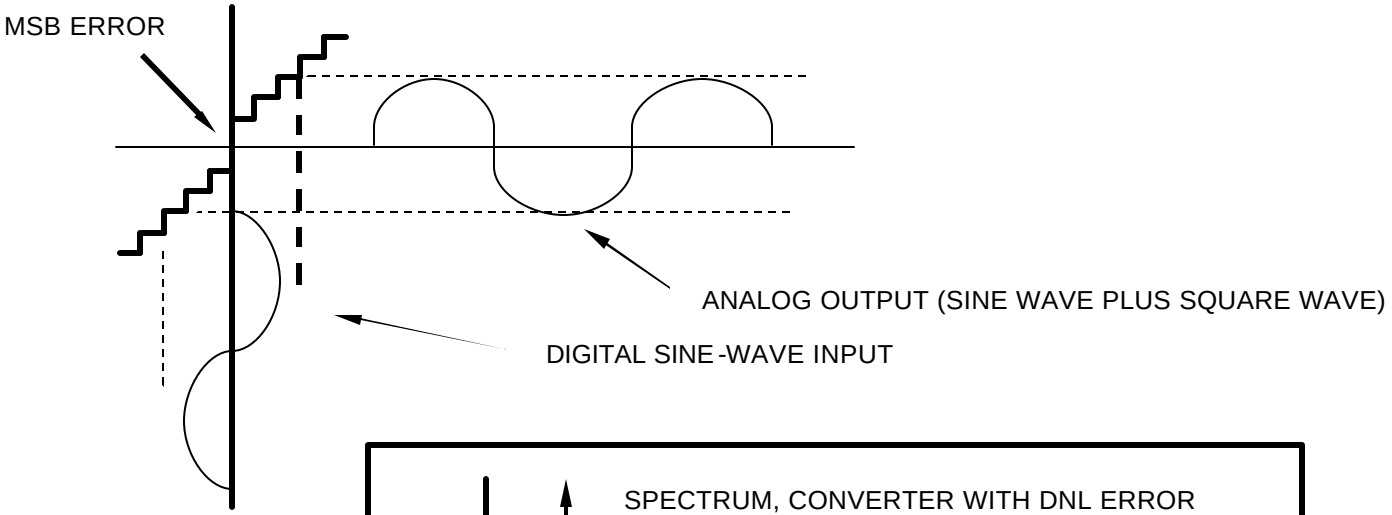


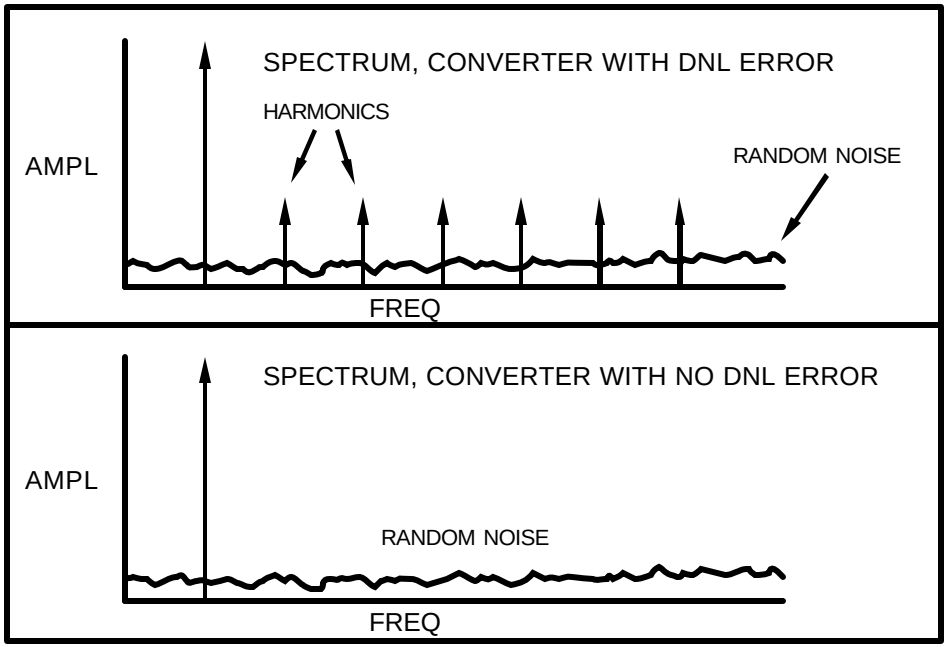
Successive-Approximation Converter with DAC Errors



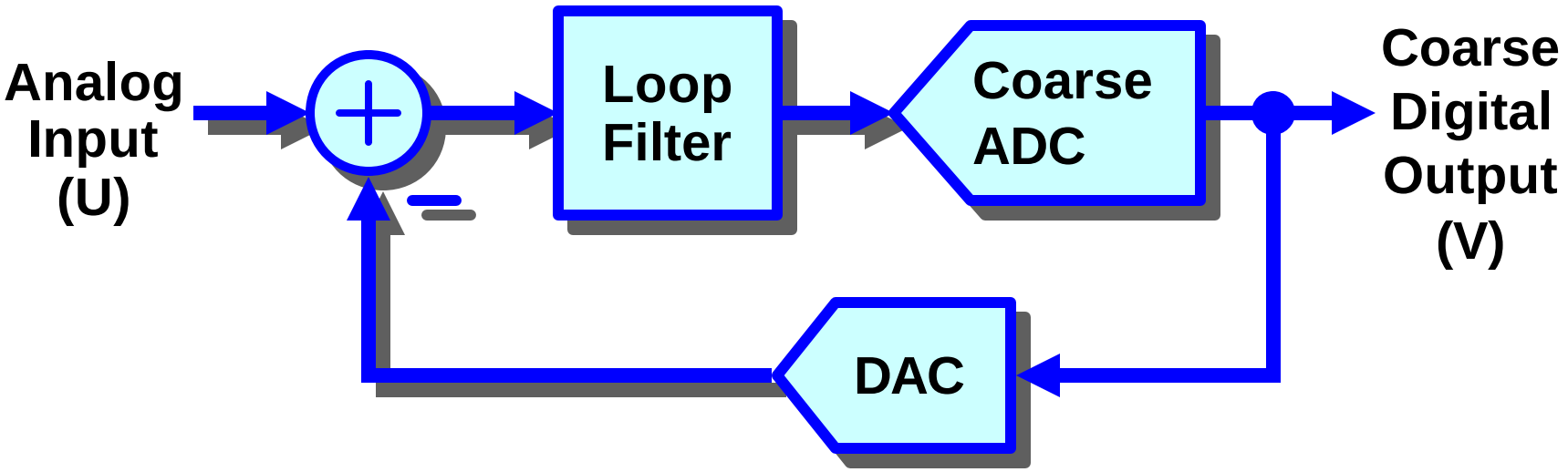


Low-Level Signal Performance of SAR Converter vs. Sigma-Delta Converter



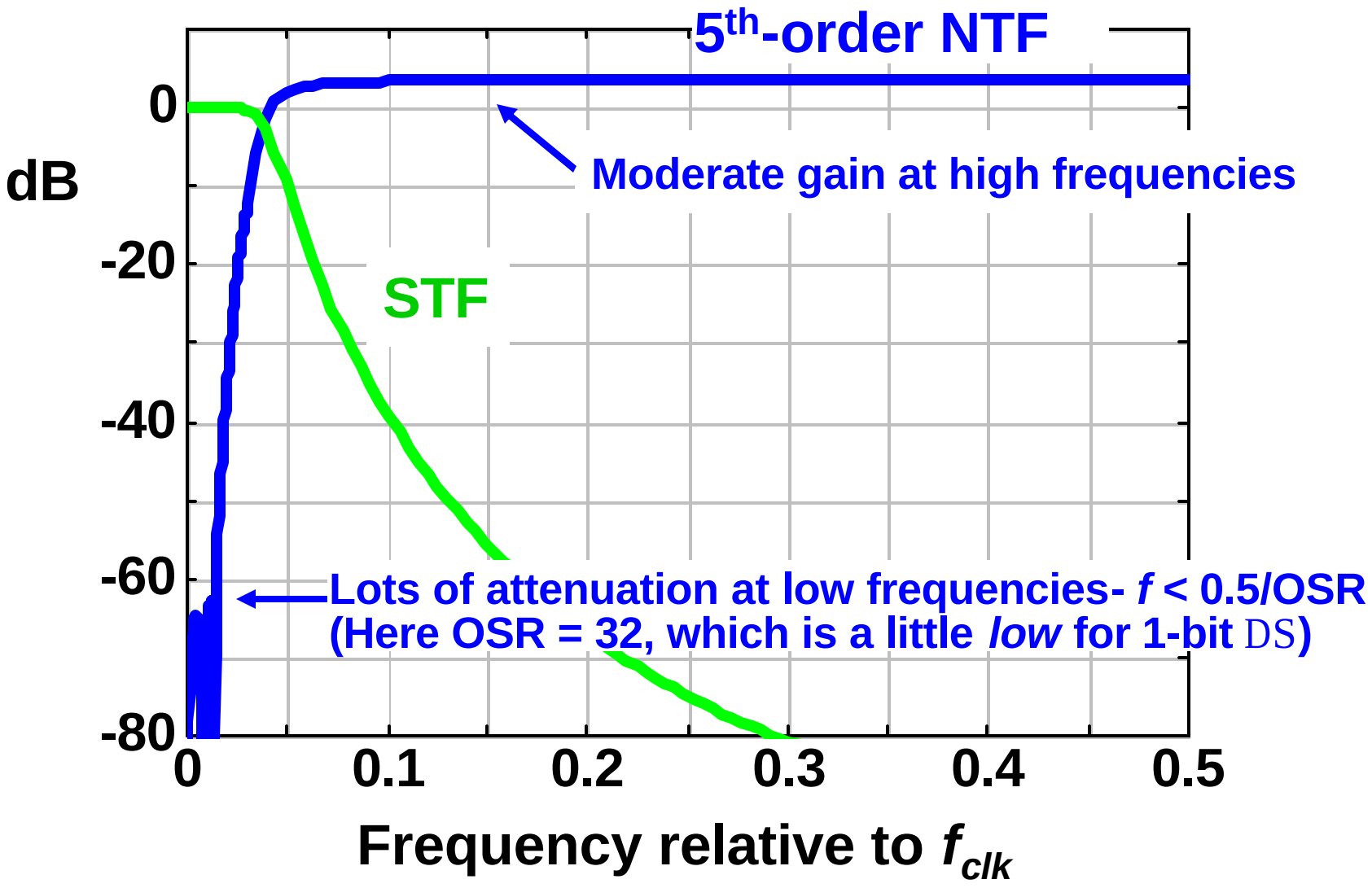


Typical Structure for Sigma-Delta ADC

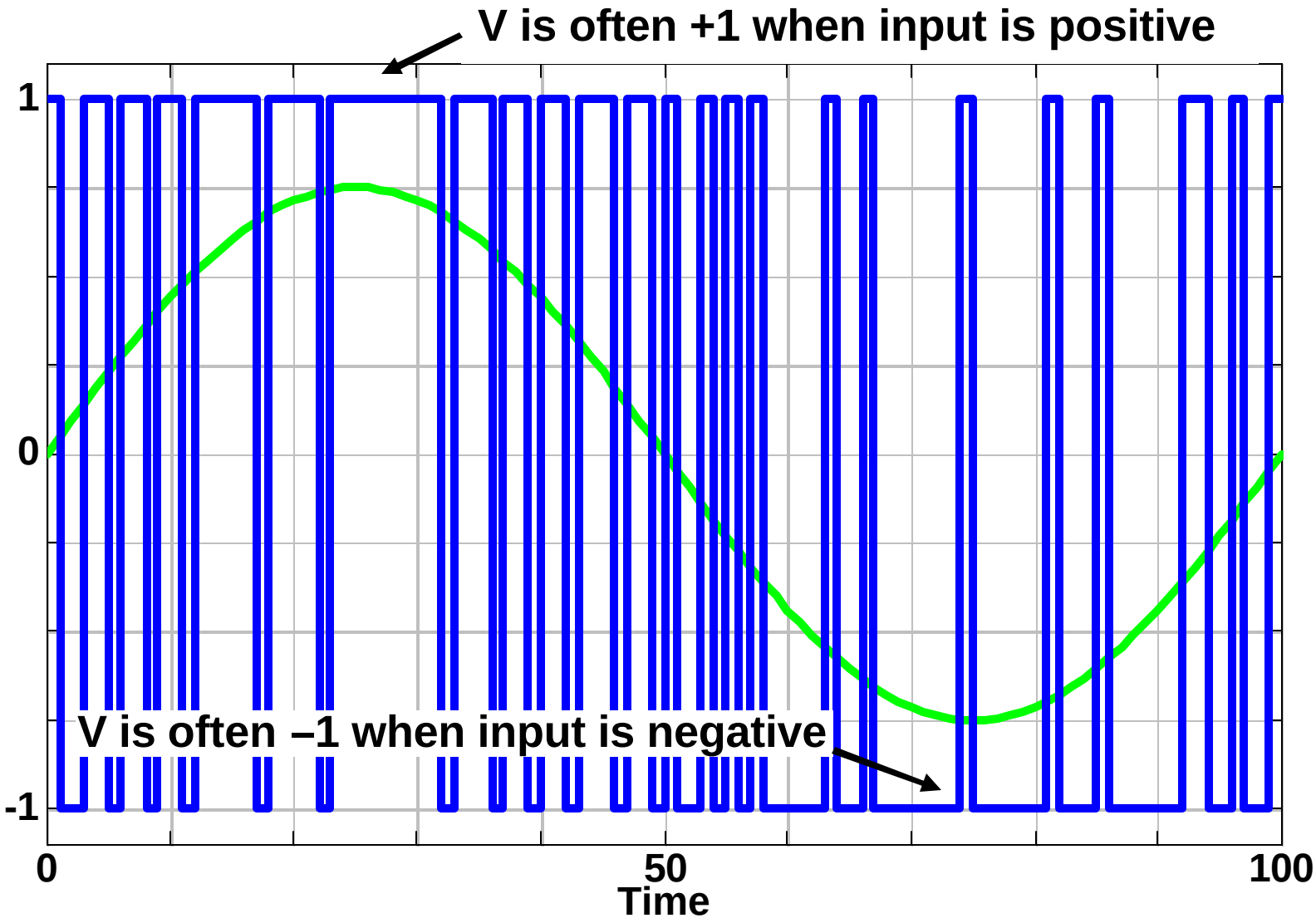


- ΔΣ makes highly-linear ADCs and DACs
  - ADCs with 22-bit linearity exist!

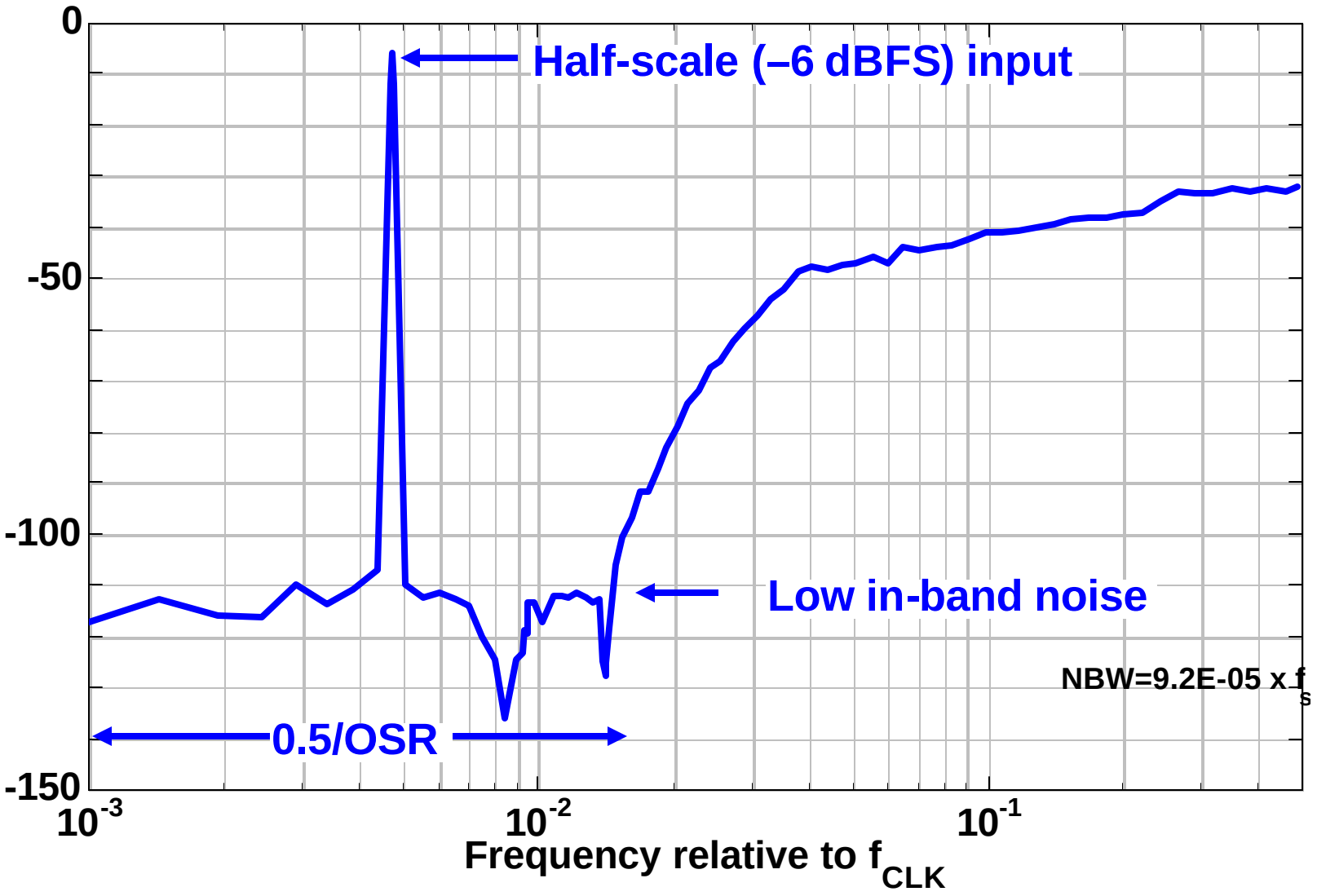
Example STF and NTF



ΔΣ in the Time Domain



ΔΣ in the Frequency Domain

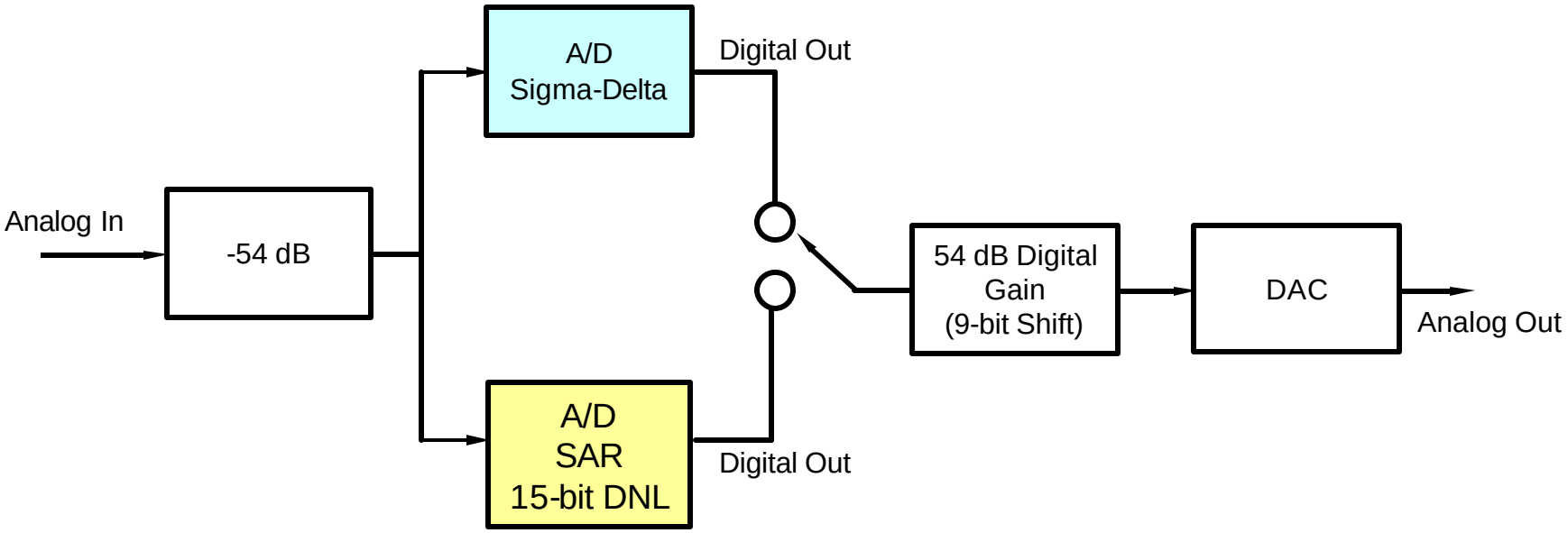


ANALOG DEVICES

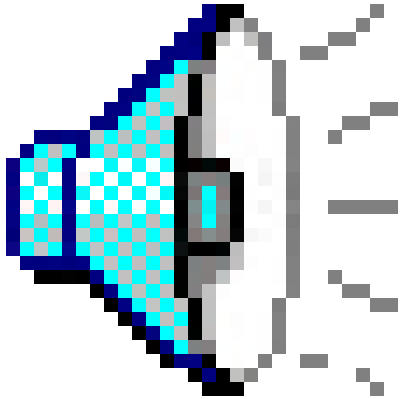
ΔΣ Basic Facts

- ΔΣ works by oversampling, coarse quantization and noise-shaping
- High SNR is possible, if OSR and modulator order are high enough
- Low-order modulators (i.e.1st-order and 2nd-order) are susceptible to in-band tones and DC-input deadbands
- Single-bit modulators are *inherently linear*, but multi-bit modulators have *much higher* performance
  - Single-bit modulators typically overload for inputs > –3dBFS
- ΔΣ modulators come in many flavors: single-bit/multi-bit, single-loop/multi-loop, lowpass/bandpass and real/quadrature (complex)

Audio Demo Setup

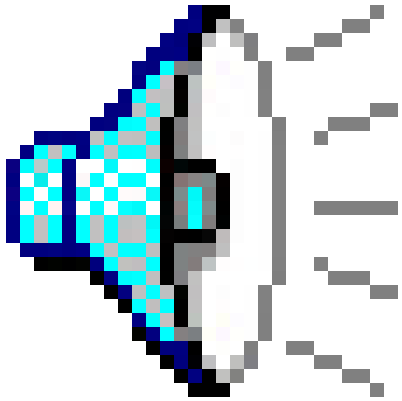


Audio Demo Setup



Sigma-Delta

Audio Demo Setup



15-bit DNL SAR

Driving Forces for New Sigma-Delta Algorithms

- A/D and D/A converters must live in a Noisy Digital Environment and still give High Performance
  - Switch from single-bit to multi-bit quantization
  - Switch from discrete-time to mix of continuous-time/discrete-time circuits
- Supply voltages are shrinking (5v -> 3V -> 1.8v -> ….)
- Digital circuits shrink MUCH more rapidly than analog circuits as process geometries decrease
  - Lots of smart DSP can be applied to fix up sloppy analog circuits
  - The only think which cannot be fixed is thermal noise!
- Consumer gear is getting smaller
  - Surround-sound A/V equipment must deliver 8X100 watts in a small space with no large heat-sinks
  - “Power-sigma-Delta” can dramatically increase efficiency and reduce heat.

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  - Split Noise-shaping – noise-shaped segmentation
  - CT DACs
  - Mixed CT/DT ADCs
- Power Sigma-Delta ("class-D" amplifiers)
  - Using dynamic hysteresis to reduce the output transition rate
- Research work
  - Multiplying Two 1-bit signals and getting a noise-shaped result
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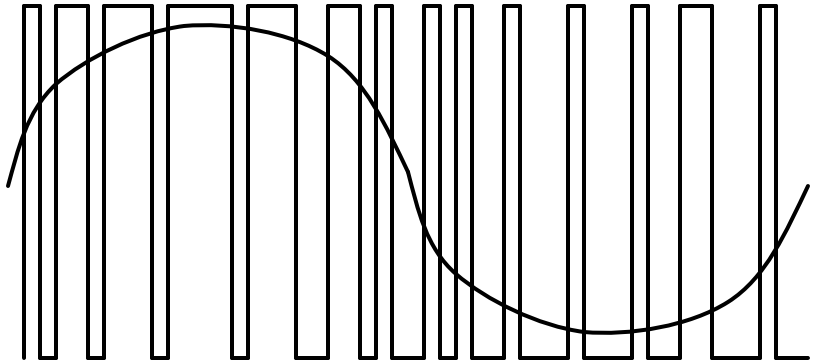
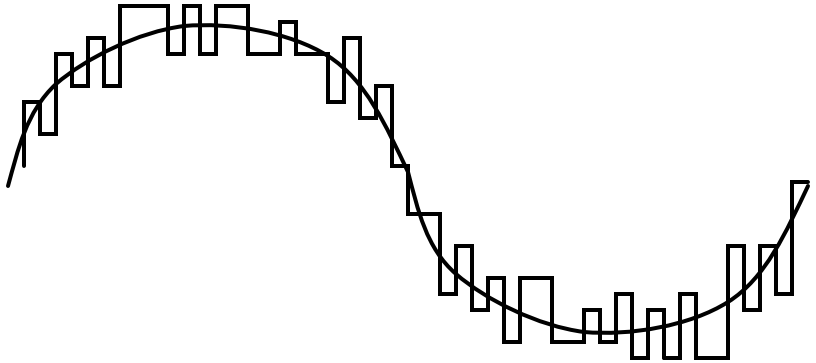
  - Noise-shaping and Prime Numbers

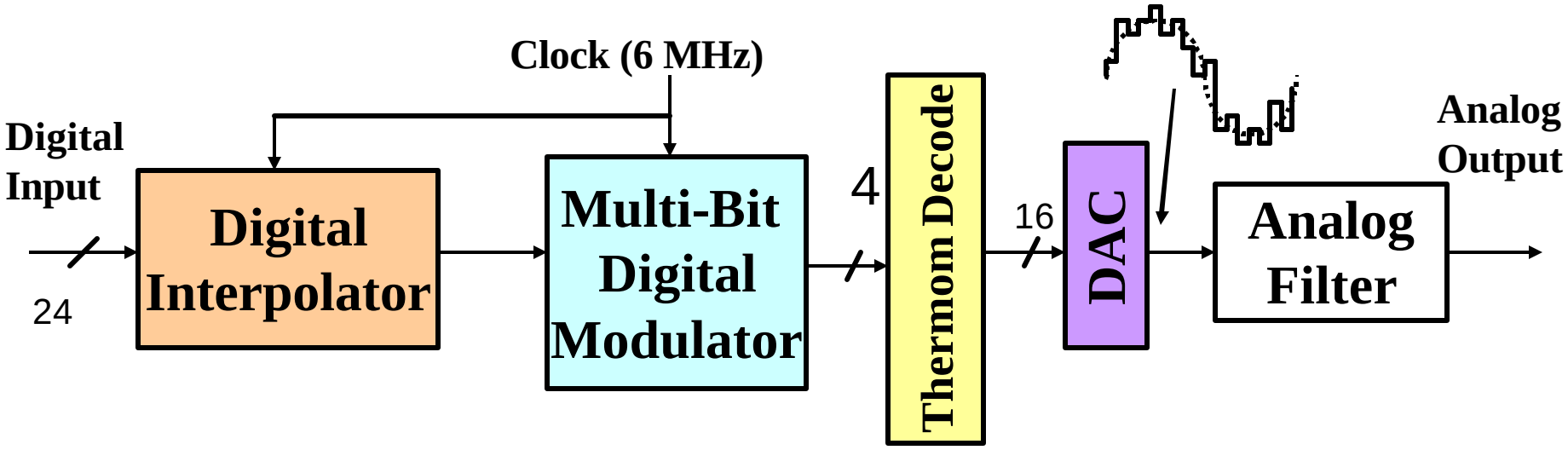
1-Bit, Multi-Bit Waveforms





- 1-bit Advantages
  - Linear – no matching
- 1-bit problems
  - Large steps (jitter sensitivity)
  - Tonal quantization noise can cause “idle tones” (quantizer can’t be dithered properly)
  - High-order loops become unstable with large inputs
- Multi-bit advantages
  - Tone-free quantization noise (can be dithered)
  - Lower-order loops can often be used (easier stability)
  - Small steps (low jitter sensitivity, less filtering required)
- Multi-bit problems
  - Matching; DAC element errors cause distortion + noise

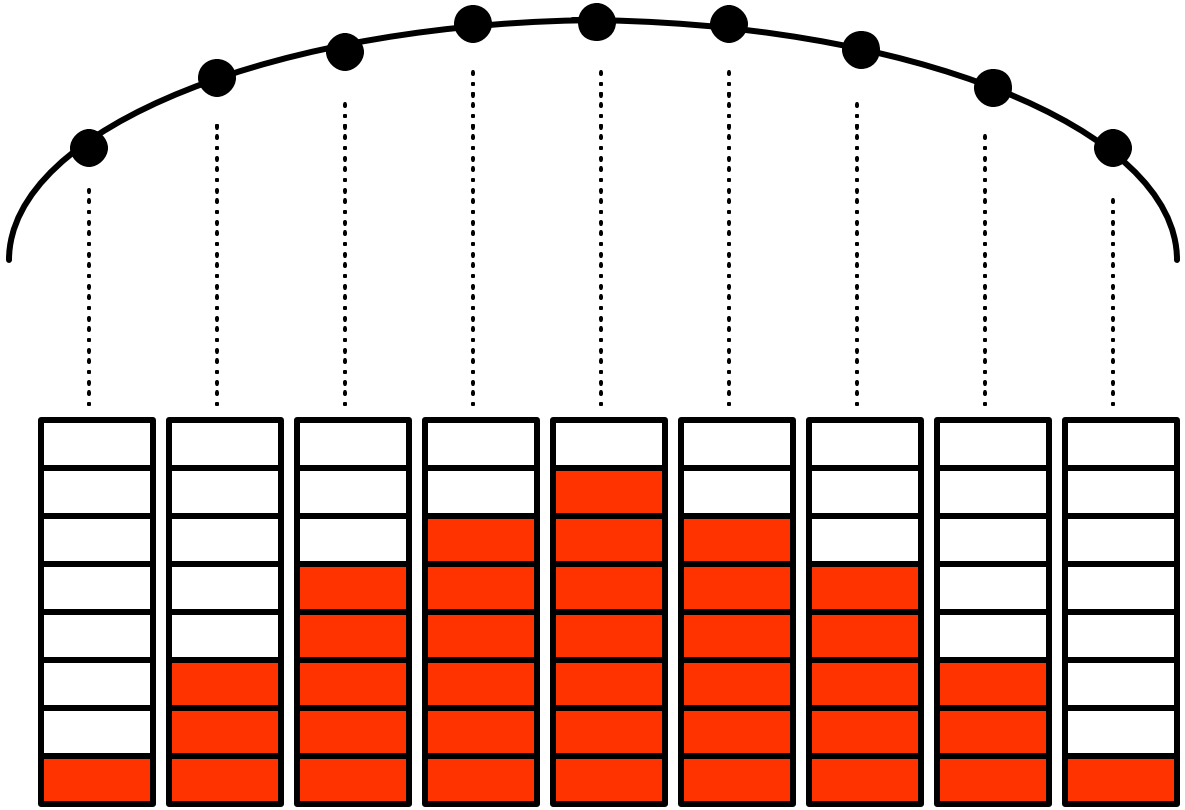
Typical Sigma-Delta DAC with Multi-Bit Continuous-Time Output Stage



- DAC is made from equally-weighted elements (resistors or current-sources)
- Analog Mismatch causes some levels to be weighted incorrectly. This causes distortion and noise.

“Thermometer Code” (3-bit example)

INPUT



OUTPUT

(after quantization and thermometer encoding)

Note; all bits are weighted equally

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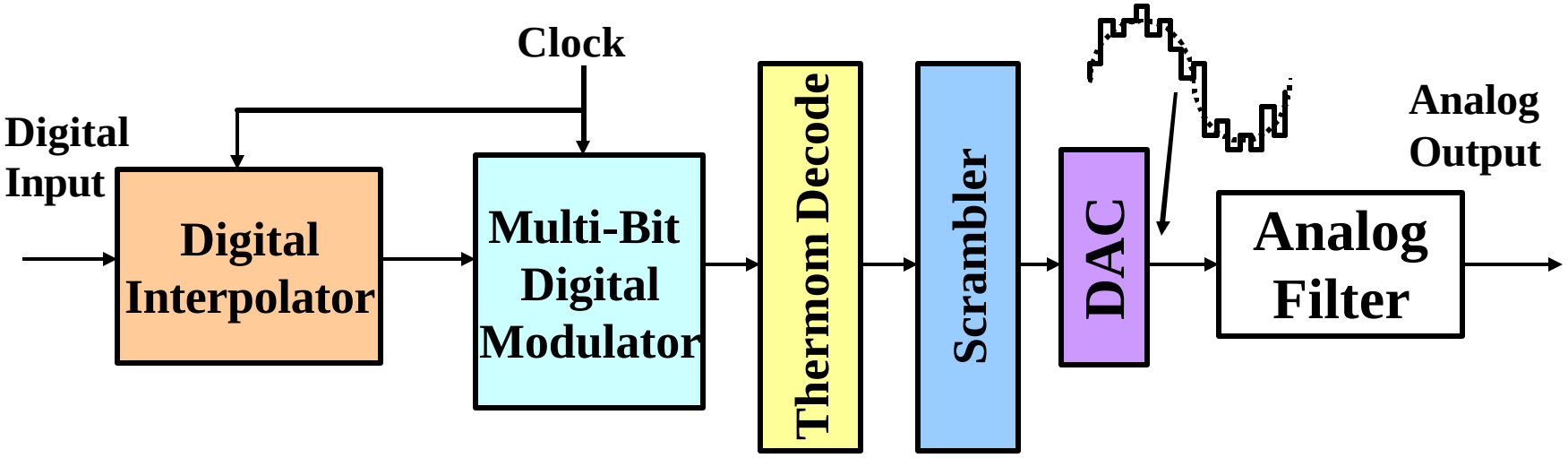
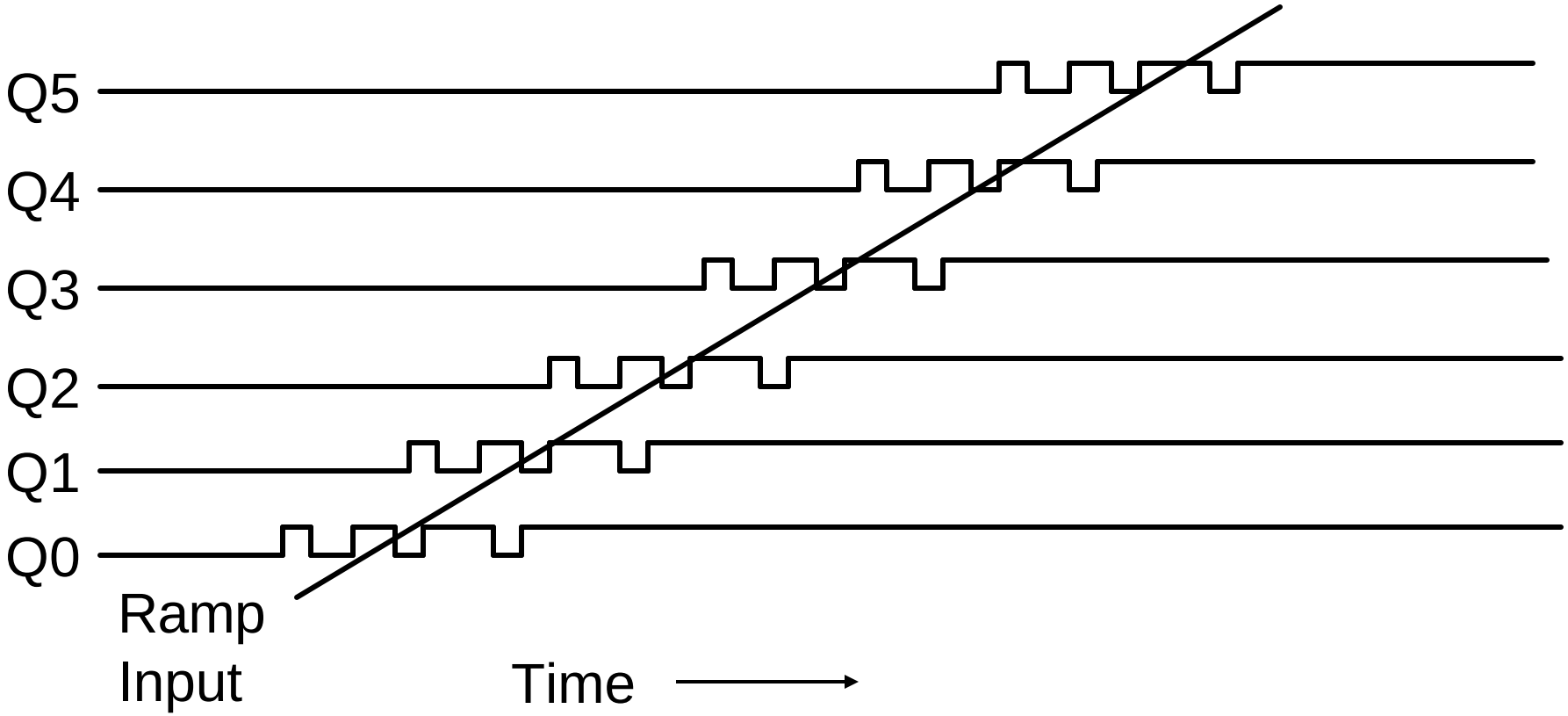
Sigma-Delta DAC with Multi-Bit Scrambled Continuous-Time Output Stage



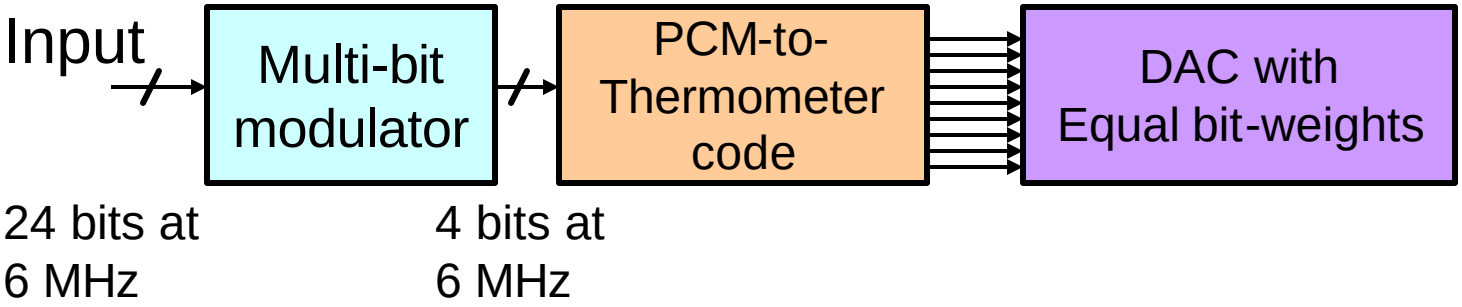
- The addition of a “Scrambler” can solve the matching problem
- The “Scrambler” dynamically remaps digital control lines to analog DAC elements. This is possible because all analog weights are equal.

Mismatch-Shaping DACs

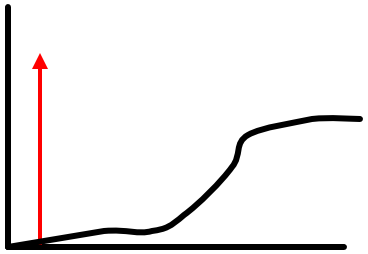
- Start by converting the PCM samples to “thermometer code”.
- All Levels Qn are weighted by the same amount.



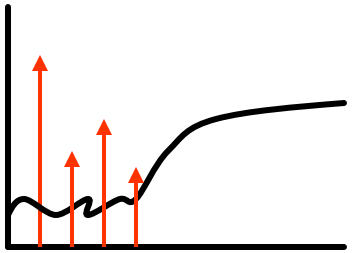
Spectral View of Mismatch Shaping



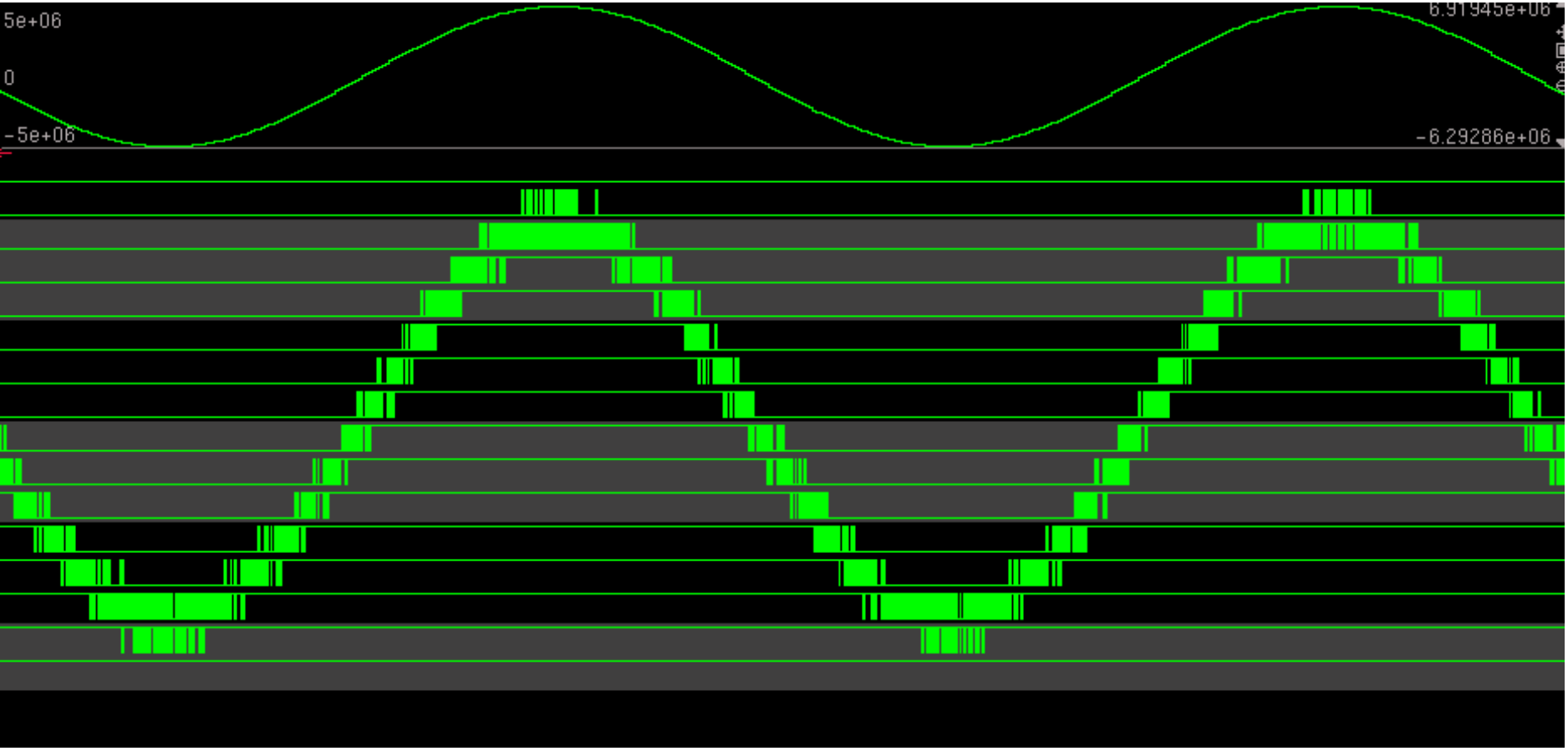
Output Spectrum with Ideal DAC



Output Spectrum with Non-Ideal DAC

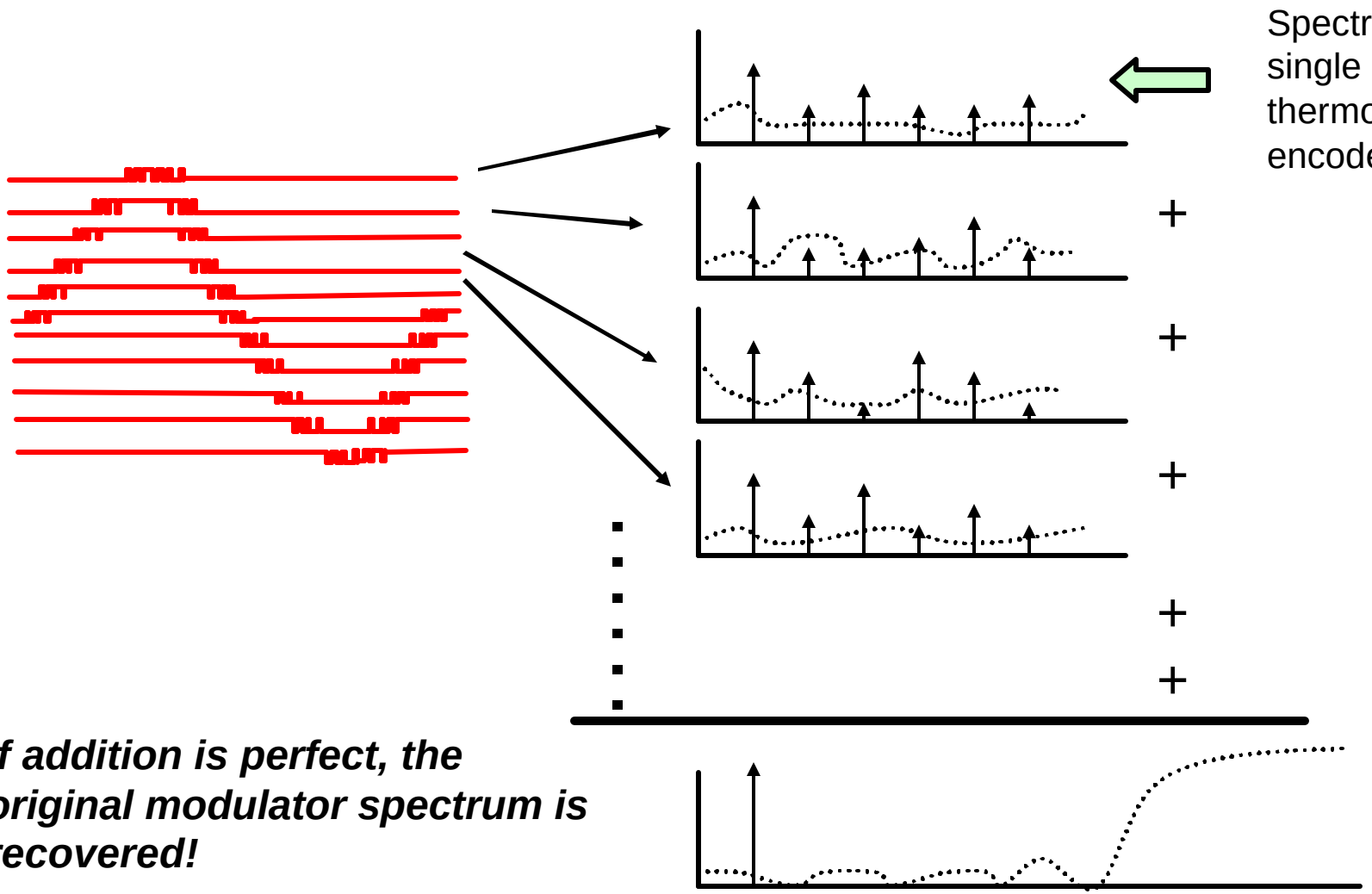


Spectral View of Mismatch Shaping



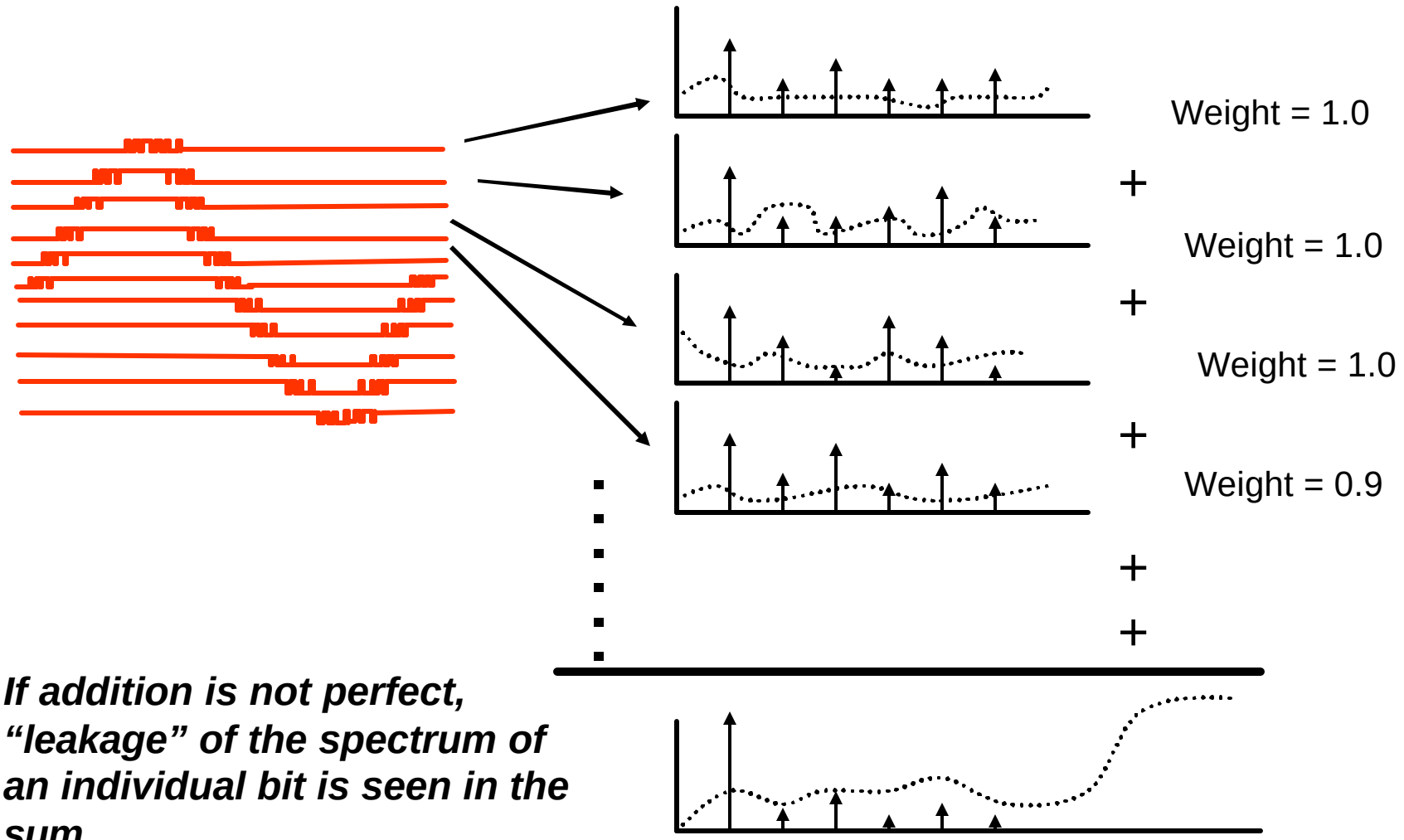
Thermometer-encoded output for sine-wave input

Spectral View of Mismatch Shaping



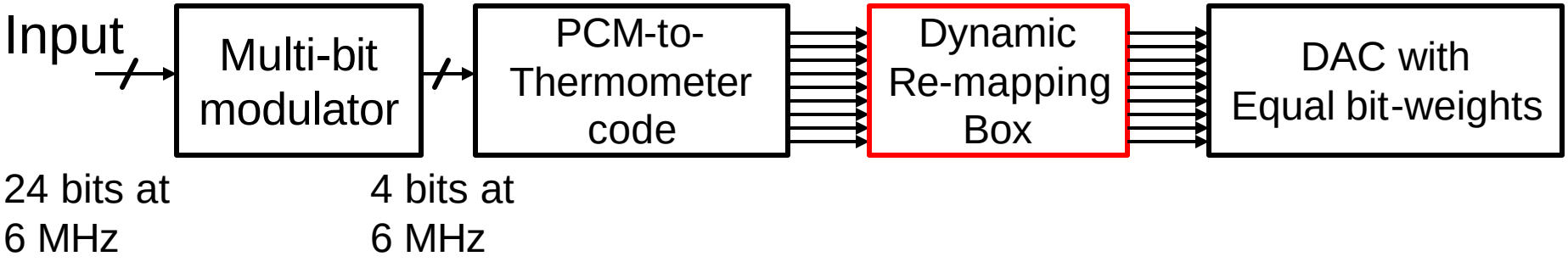
If addition is perfect, the original modulator spectrum is recovered!

Spectral View of Mismatch Shaping



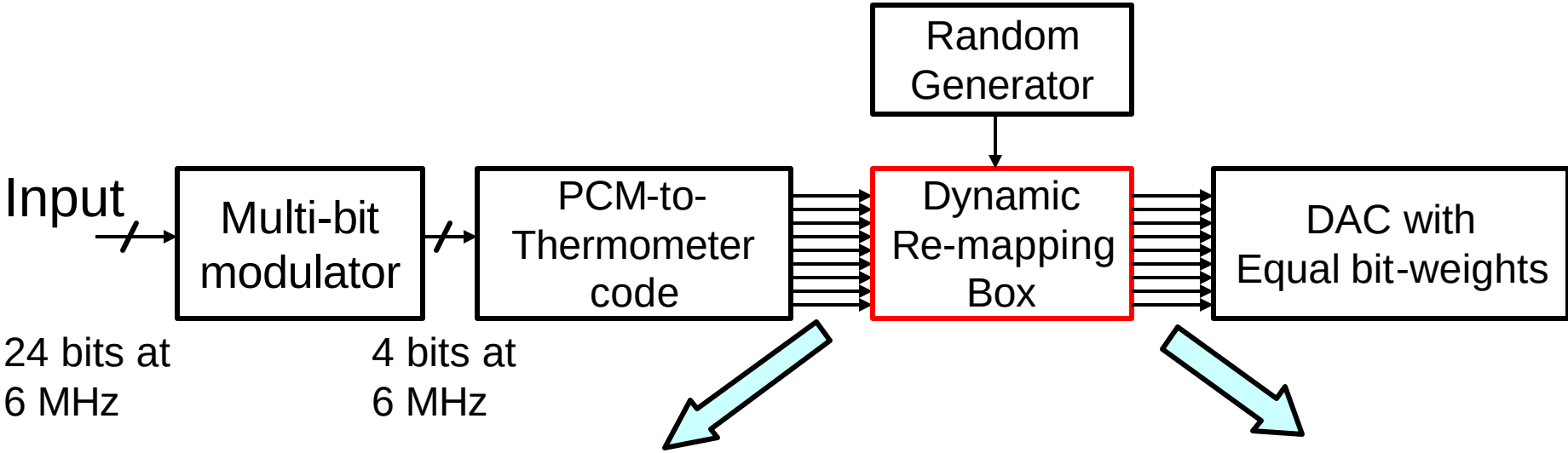
If addition is not perfect, "leakage" of the spectrum of an individual bit is seen in the sum.

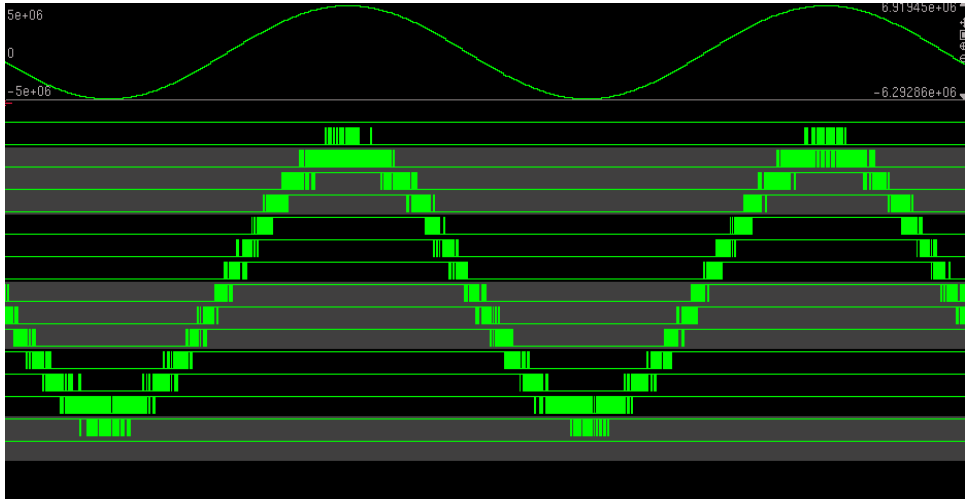
Dynamic Re-mapping (“scrambling”)

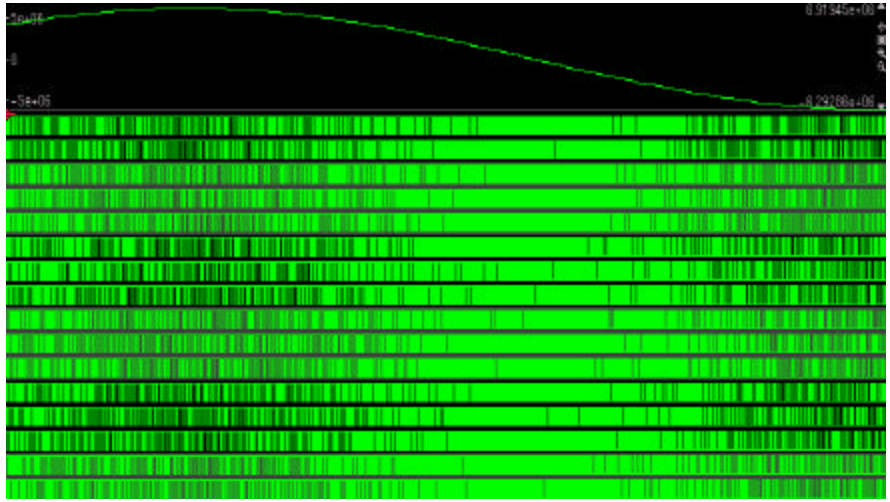


- Since the bit weights of thermometer code are equal, the mapping from digital bit to analog DAC element is arbitrary and can be changed “on-the-fly”.
- Random re-mapping turns all DAC errors into white noise
- Data-dependant re-mapping can turn DAC errors into shaped noise!

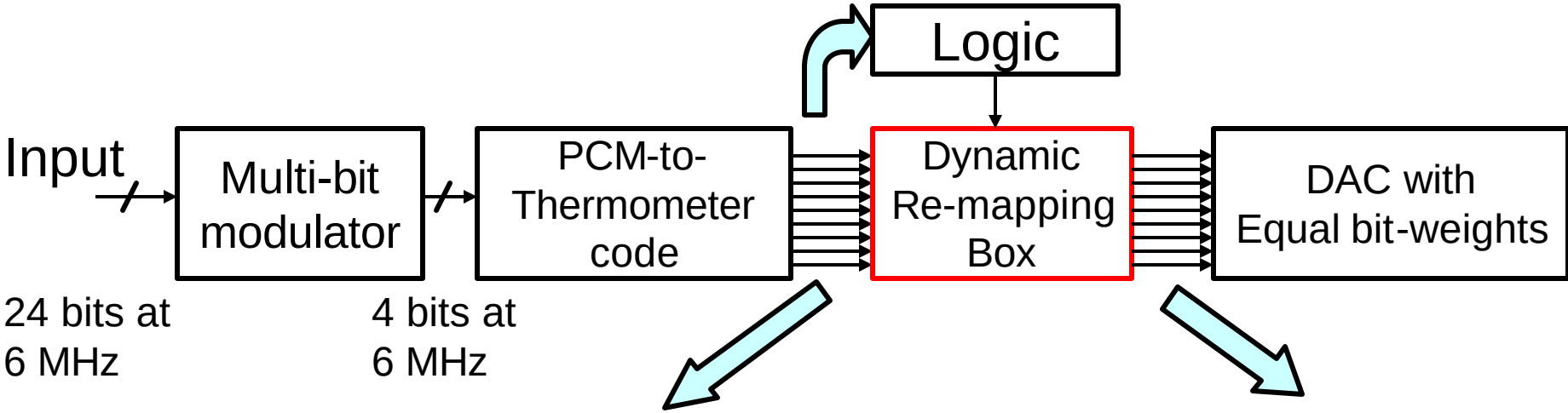
Random Scrambling

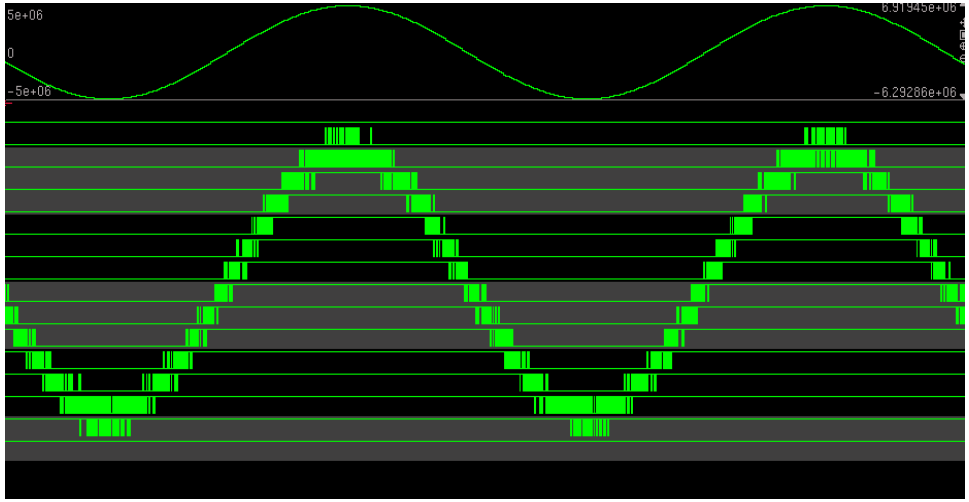


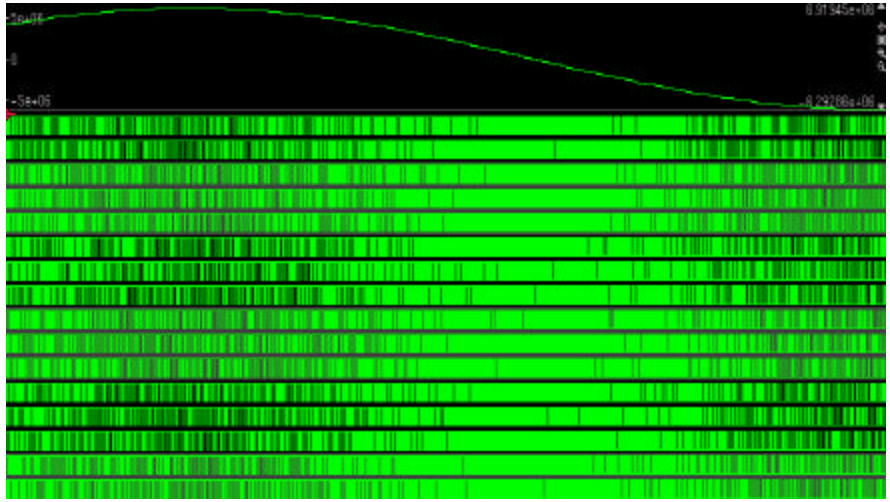




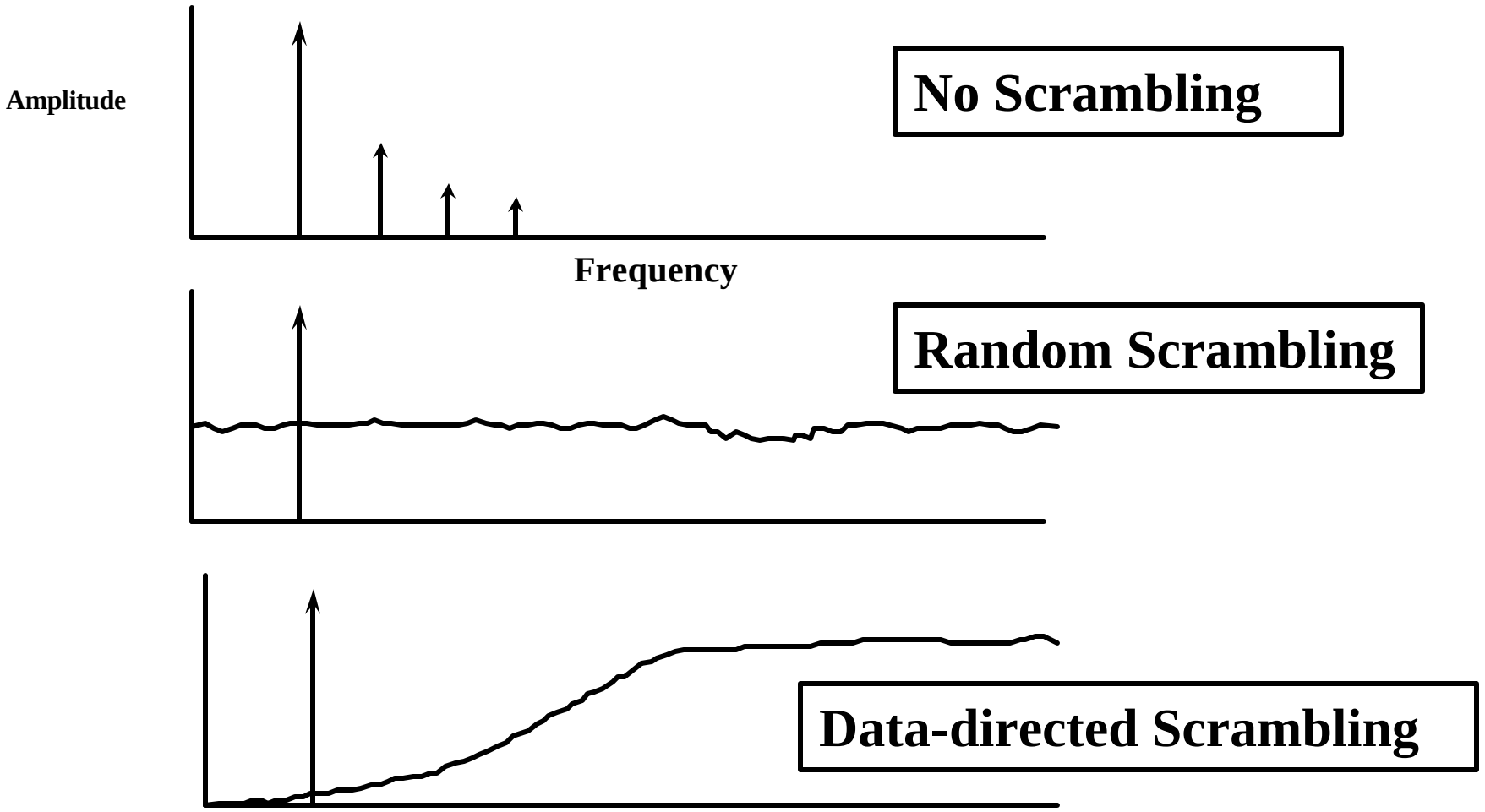
Data-directed Scrambling



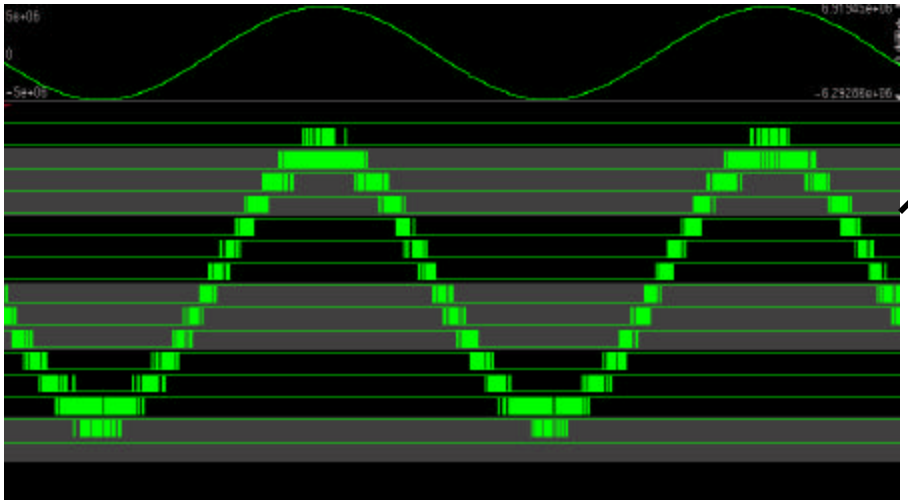


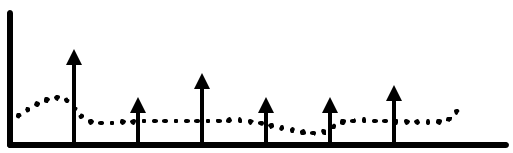


Scrambling and Element Mismatch



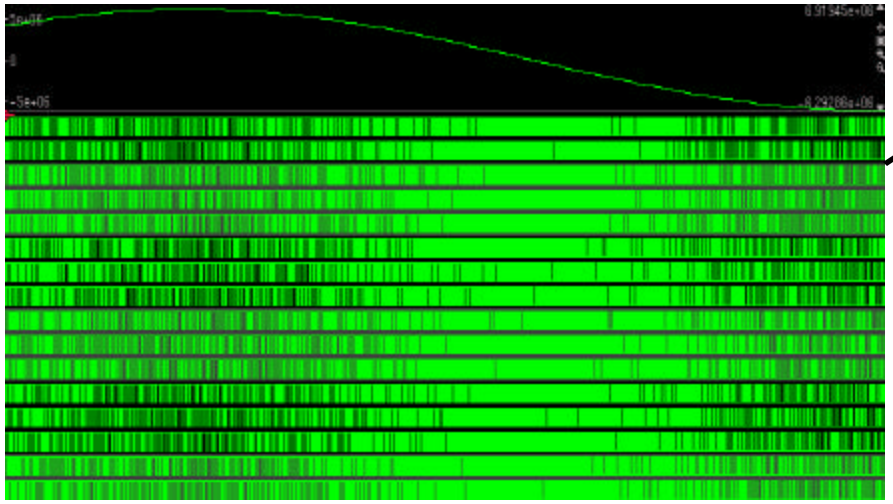
Comparison of individual-bit spectra between No Scrambling and Random Scrambling

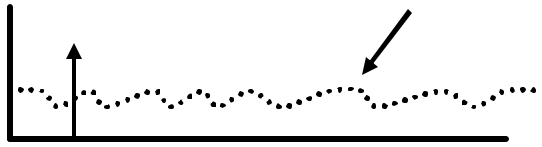




Spectrum of an Individual Bit

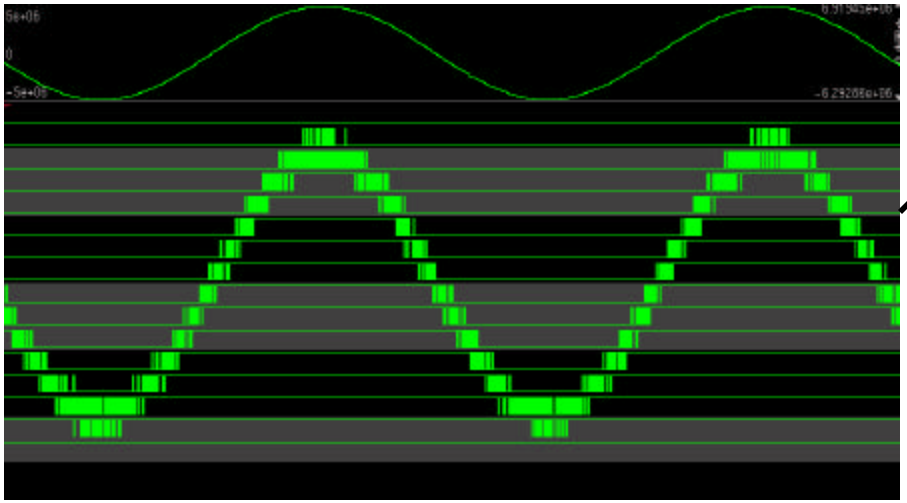
DAC errors become White Noise

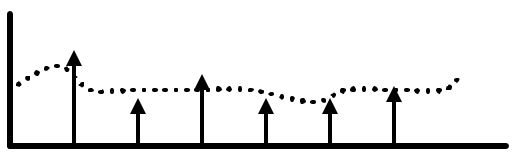




Spectrum of an Individual Bit

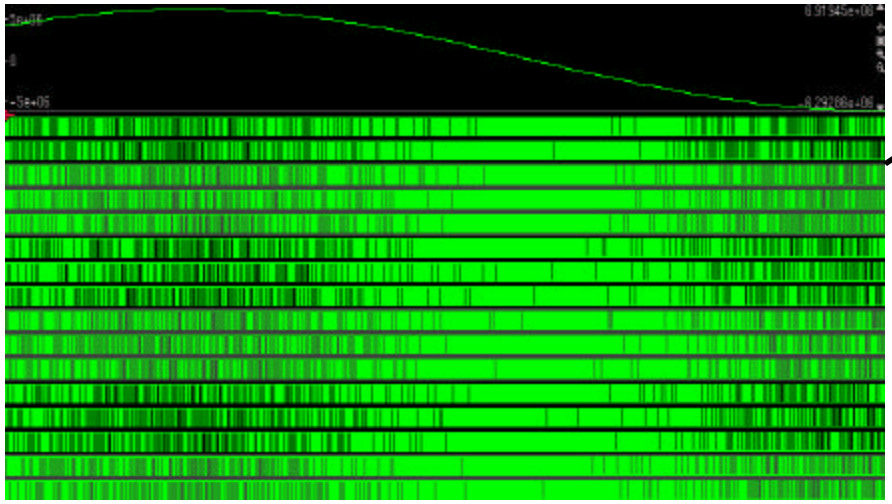
Comparison of individual-bit spectra between No Scrambling and Data-Directed Scrambling

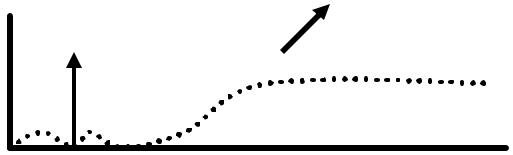




Spectrum of an Individual Bit

DAC errors become Shaped Noise

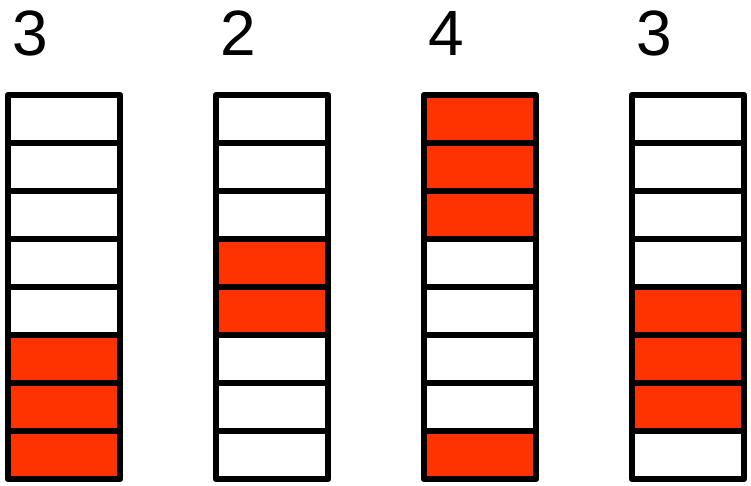




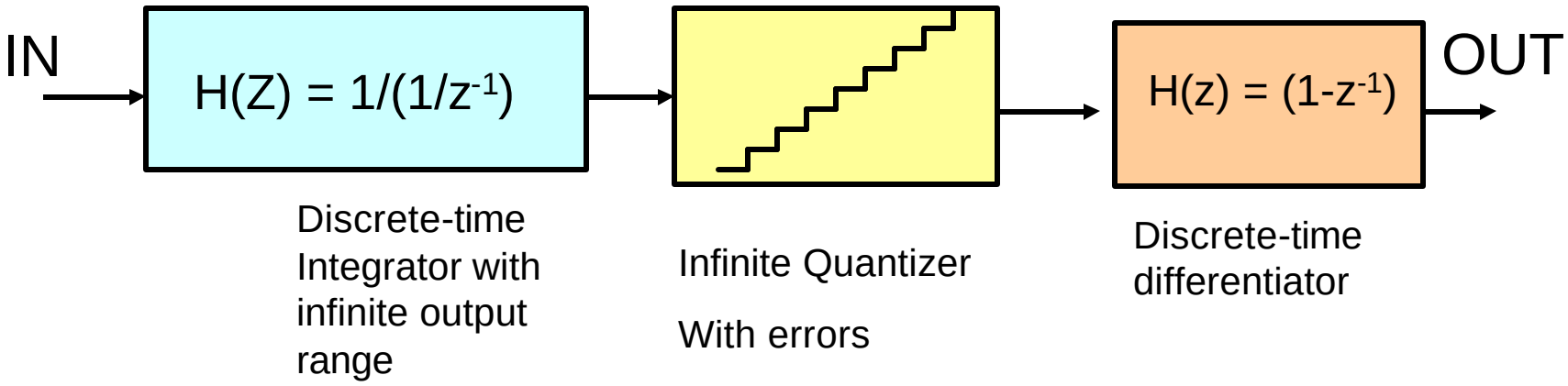
Spectrum of an Individual Bit

Algorithms for data-directed scrambling

- Rotating “start-pointer” scheme
  - New elements are turned on starting where the previously-used elements ended
  - Example – data pattern 3 2 4 3 in an 8-level system



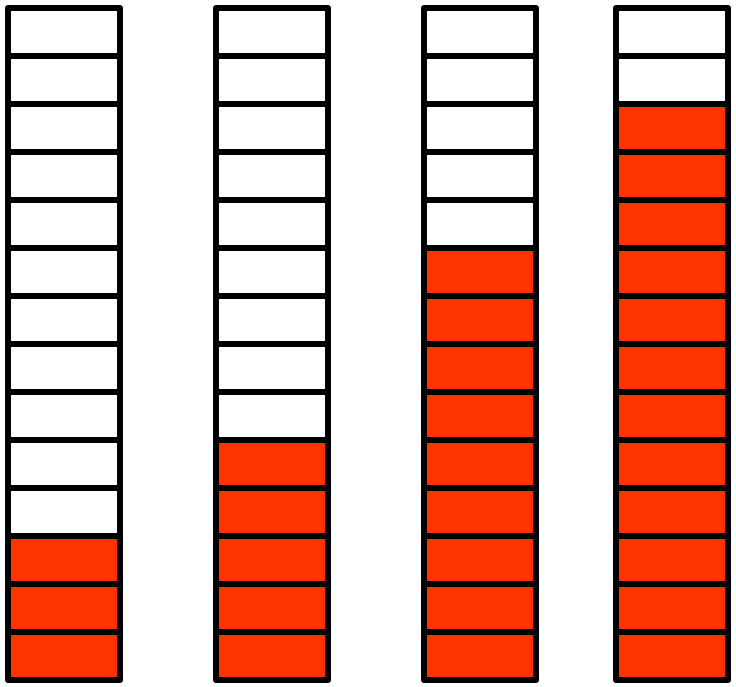
Rotating Barrel-Shifter approach; analysis



- Quantizer errors are shaped to 1st order
- Requires an infinite quantizer since the integral of an unknown signal tends towards infinity.

Algorithms for data-directed scrambling

Input →	3	2	4	3
Integral →	3	5	9	12



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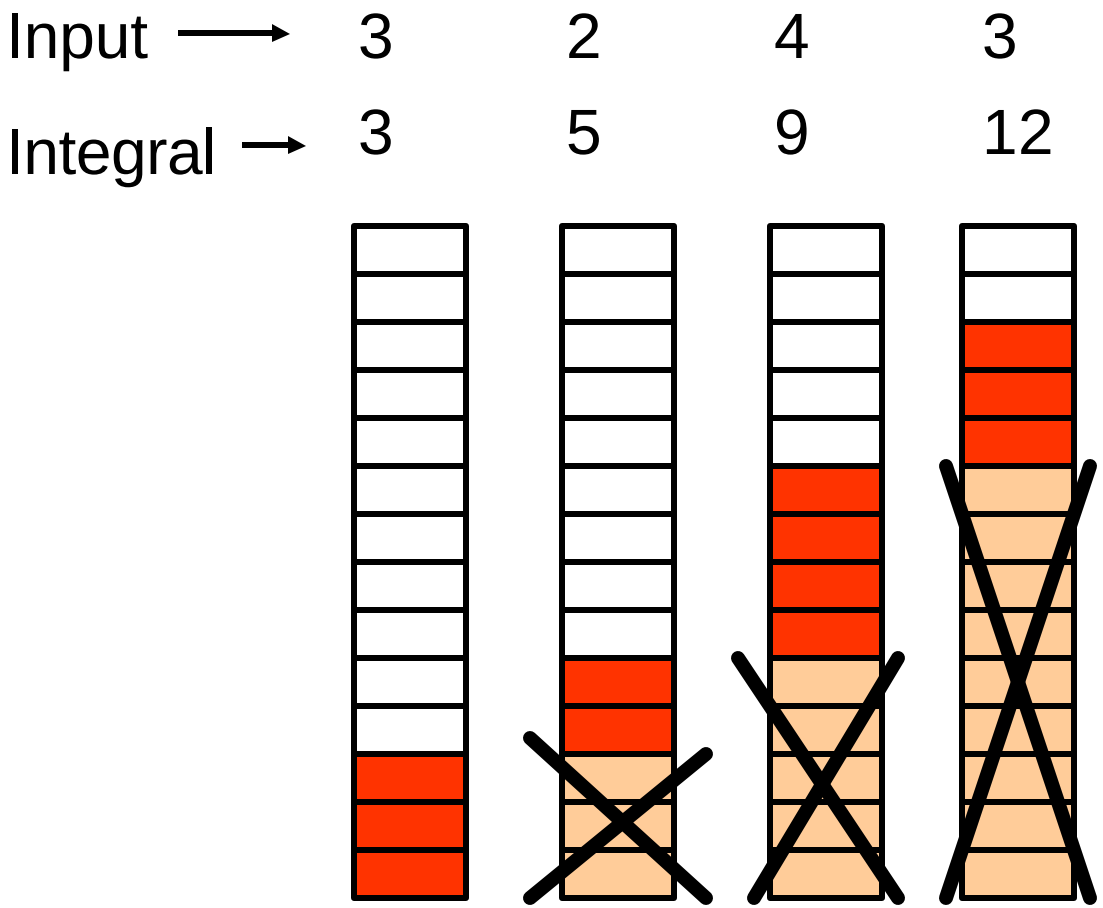
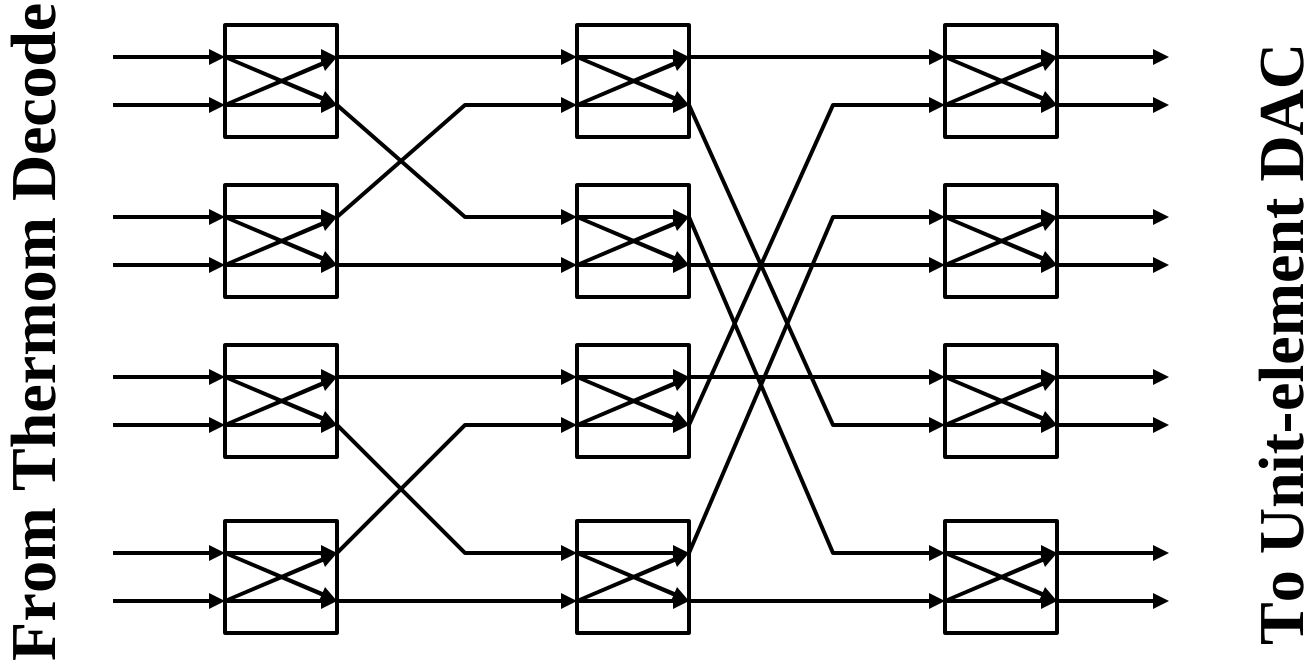


Differentiation operation of (new – old) can be done in the “thermometer-domain” by turning off the “old” bits and turning on the “new” bits starting at the end of the “old” location!

Algorithms for data-directed scrambling

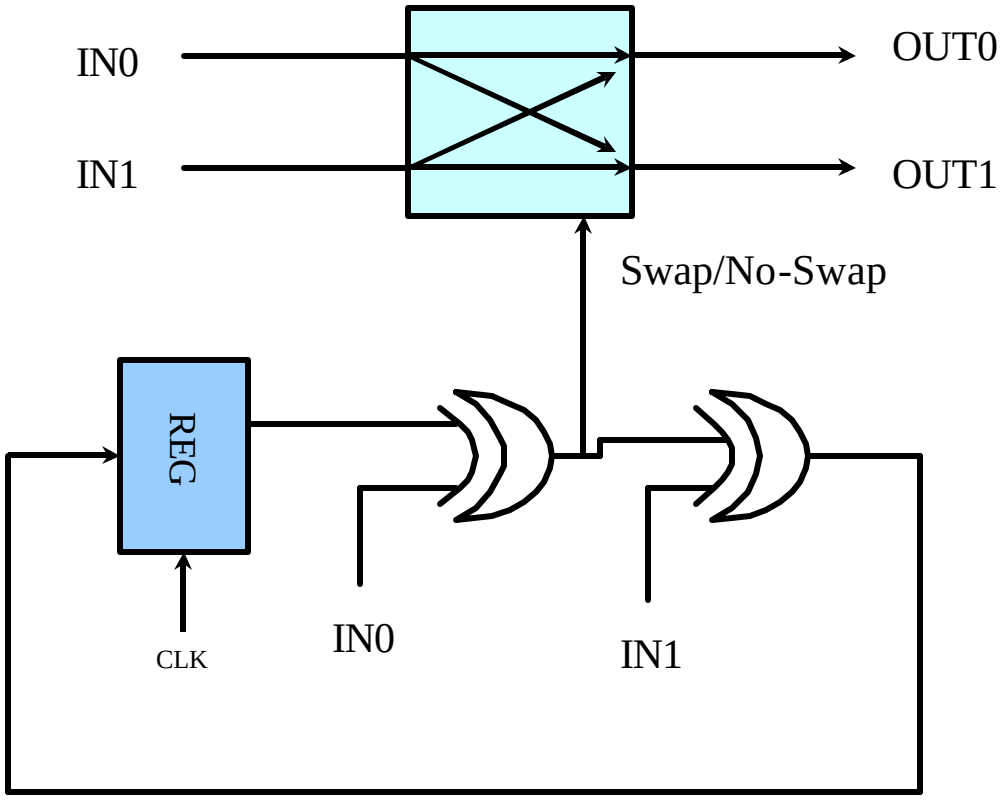
- Butterfly routing scheme
  - Every input can reach every output
  - Each local butterfly unit has its own logic to keep the “usage” between its two outputs balanced
  - Amazingly, this causes each output to contain signal + shaped noise



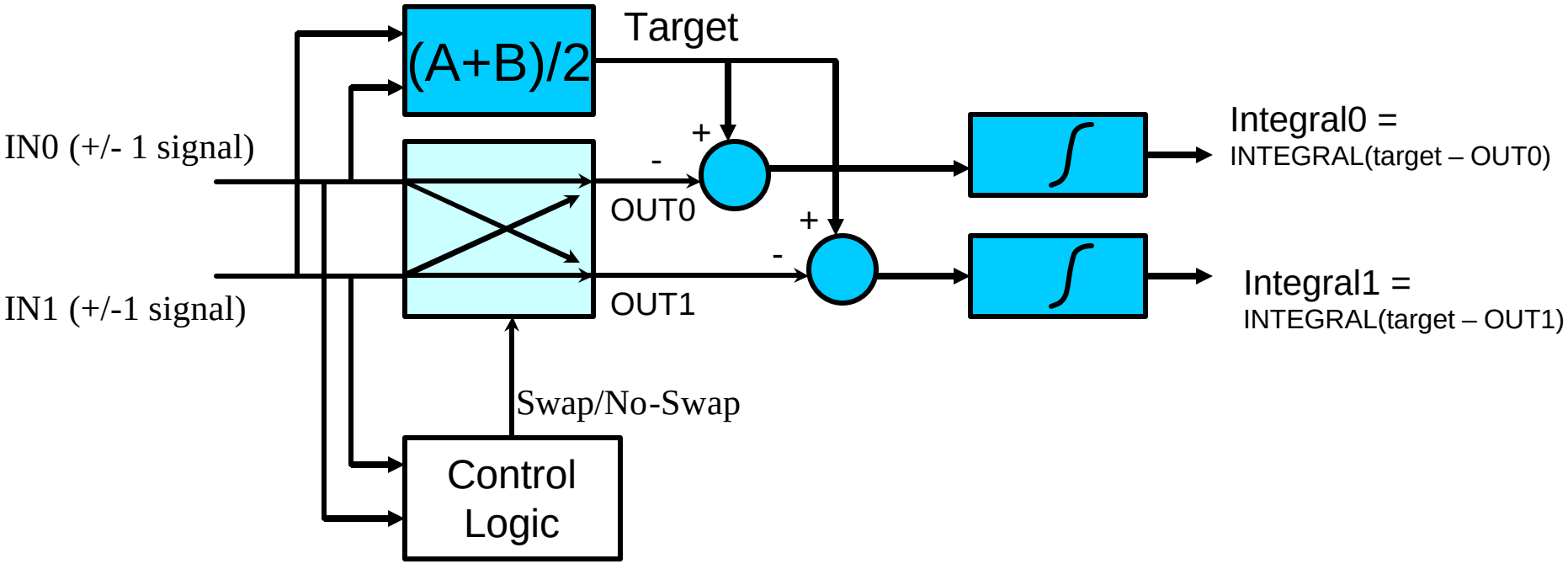
3-Bit/ 8-level Example

1996 ISSCC, Adams + Kwan

Butterfly Scrambler cell design

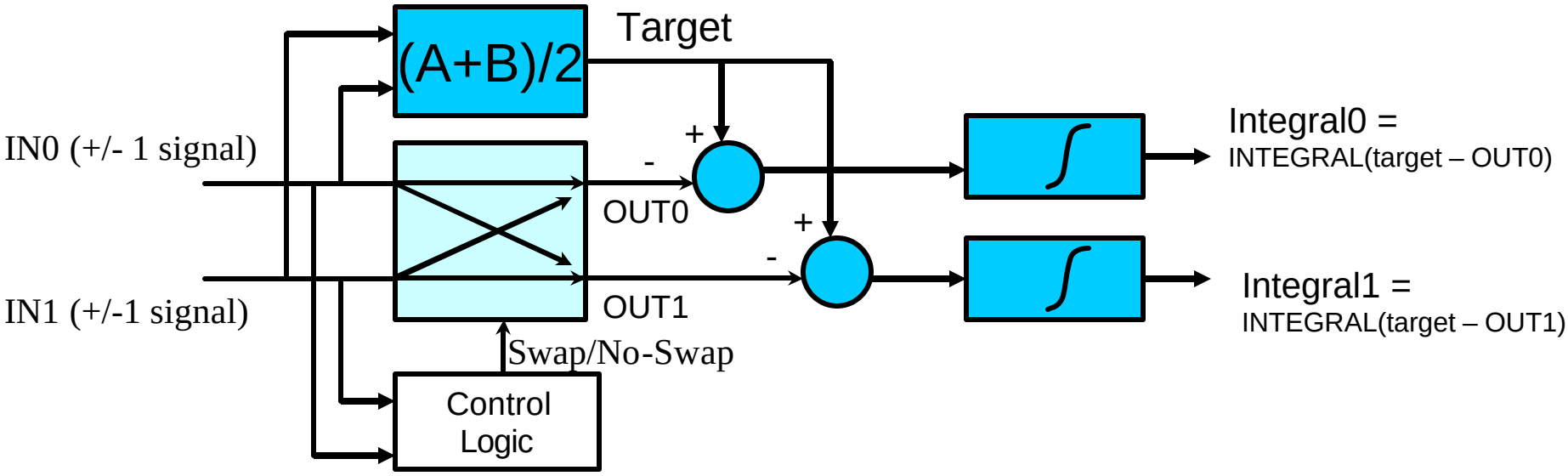


Butterfly Scrambler Theory



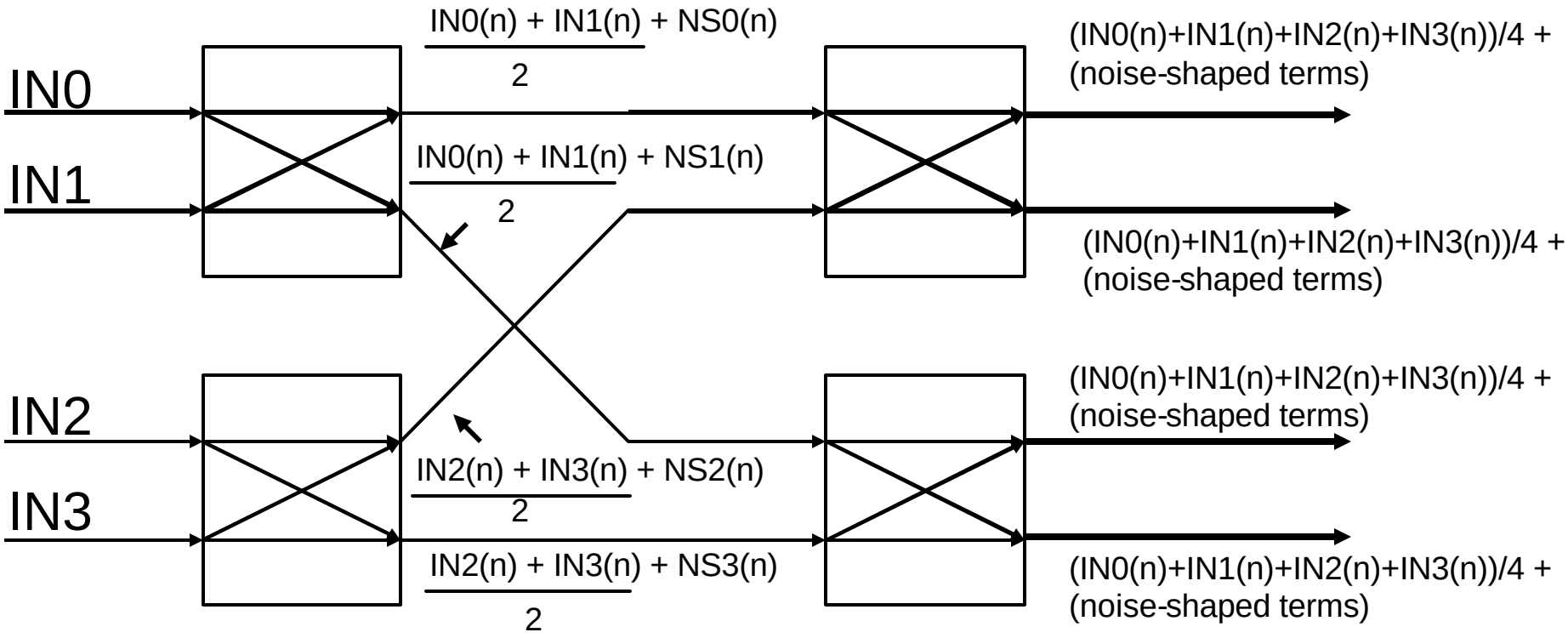
= blocks added for analysis purpose only
(not actually used in real circuit)

Butterfly Scrambler Theory



- By establishing a target which is (A+B)/2, we force the SUM of Integral1 + Integral0 to be zero
- By using the appropriate control logic, we bound the DIFFERENCE between Integral0 and Integral1 to +1/2.
- Both Integral1 and Integral2 are therefore small.
- Therefore OUT0(n) = ((IN0(n) + IN1(n))/2) + NS(n), where NS(n) is a first-order highpass noise-shaped sequence. Ditto for OUT1(n).

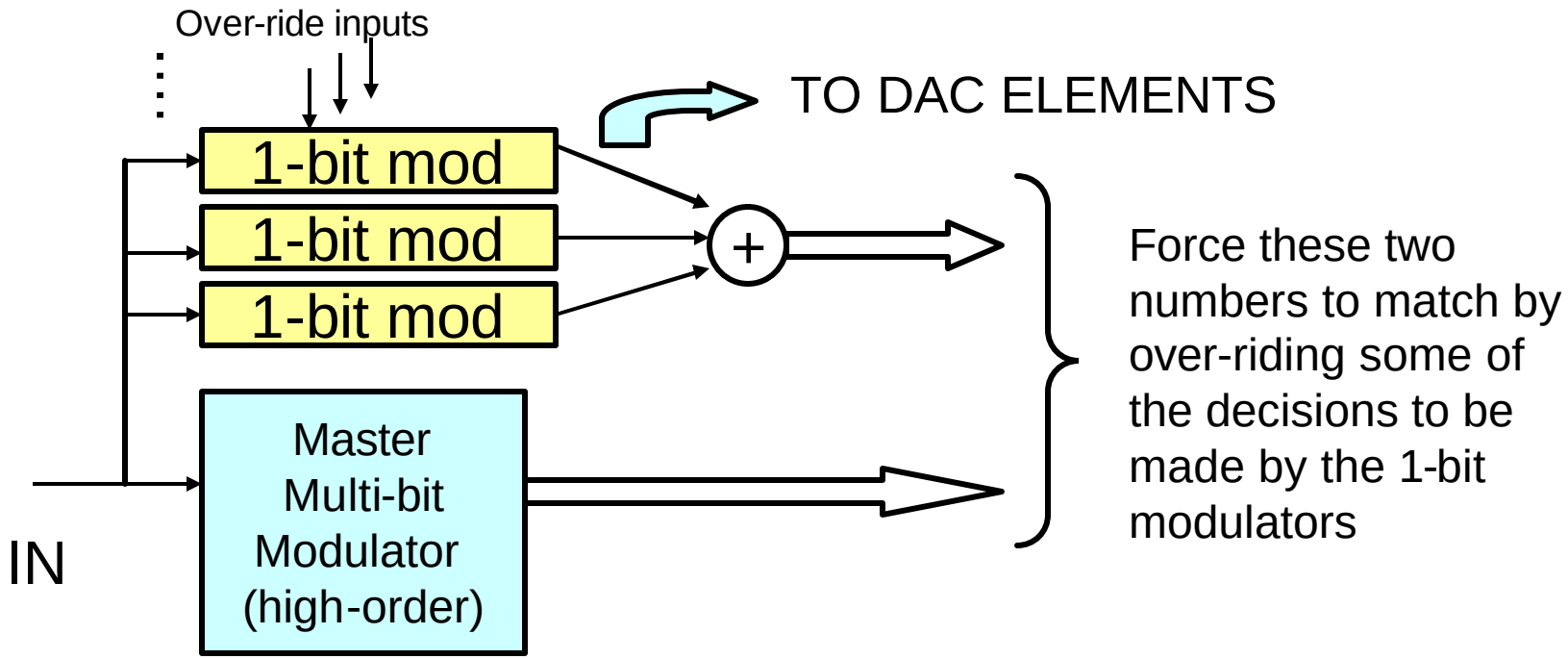
Butterfly Scrambler Spectral View



- Each output is the SUM of all the inputs plus a first-order highpass noise-shaped term
- This property extends to all larger networks as well.

Algorithms for data-directed scrambling

- Master/Slave modulator scheme
  - The sum of many 1-bit modulators is forced to match a single multi-bit modulator
  - Needs an algorithm to decide which 1-bit modulator to override.
  - 1-bit mod must be highly stable to permit over-rides without stability problems



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  - Multi-bit Mismatch Shaping
  - *Split Noise-shaping – noise-shaped segmentation*
  - CT DACs
  - Mixed CT/DT ADCs
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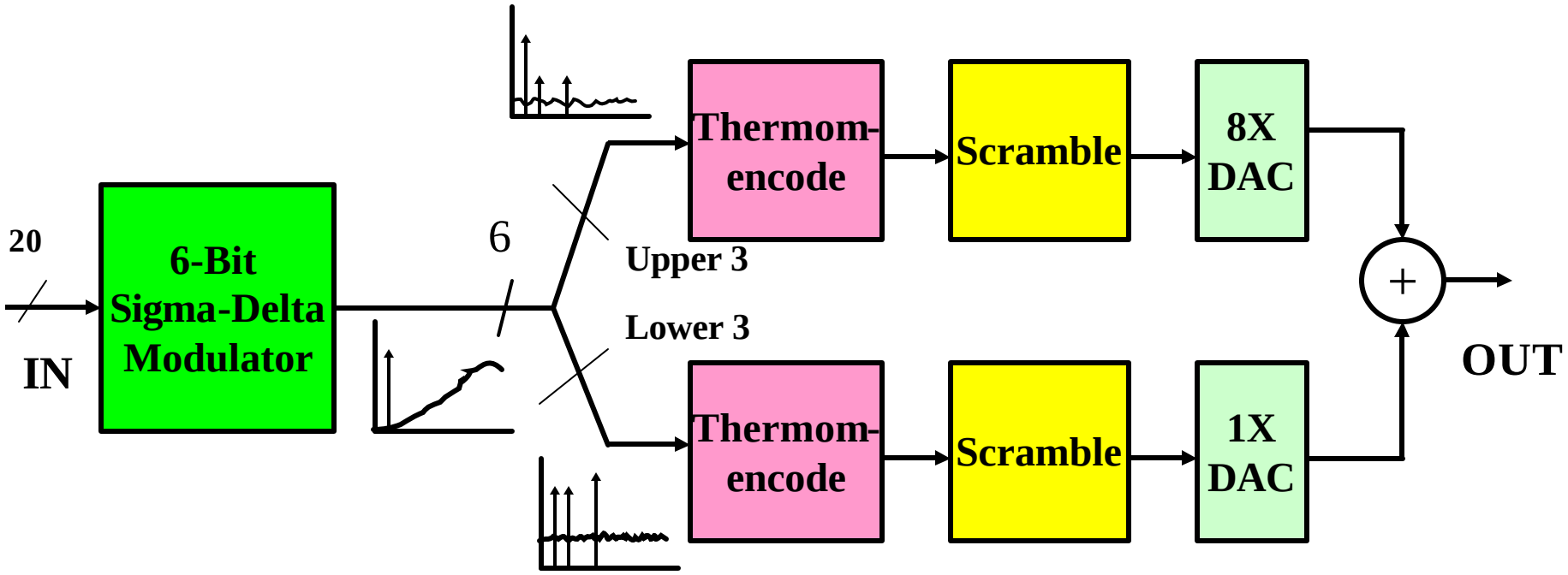
  - Using dynamic hysteresis to reduce the output transition rate
- Research work
  - Multiplying Two 1-bit signals and getting a noise-shaped result
  - Single-structure sigma-delta/successive-approximation; a converging time-domain view of sigma-delta
  - Noise-shaping and Prime Numbers

Noise-Shaped Segmentation

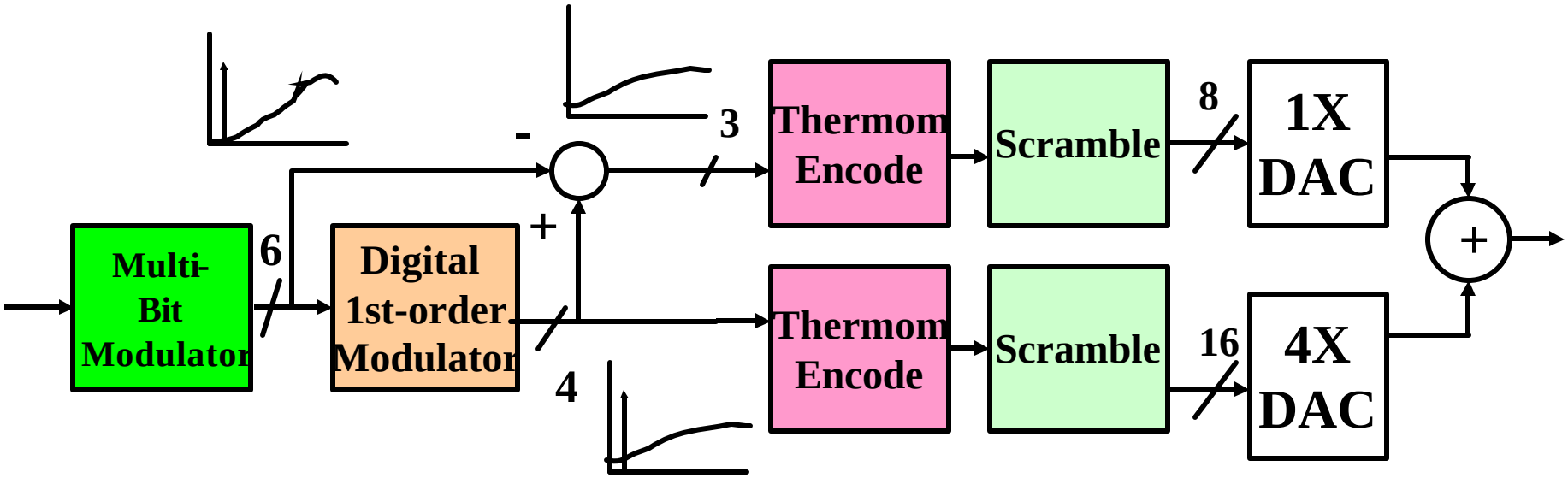
- The problem with thermometer code …
  - # of DAC elements grows by 2^N for an N-bit PCM signal
- Solution #1 – break up PCM bus into sub-sections, scramble each section individually and apply to two separate DACs
  - Problem; inter-DAC errors not shaped
- Solution #2 – use a noise-shaping “splitter” algorithm to construct two noise-shaped signals whose sum equals the original modulator signal. Apply to two separate DACs
  - Order of noise shaping for the “splitter” can be lower than that of the main modulator.

Segmentation, the wrong way



- **Errors in the 1x DAC are noise-shaped**
- **Errors in the 8X DAC are noise-shaped**
- **Gain errors between the 1X DAC and the 8X DAC are NOT shaped!**

Noise-Shaped Segmentation



- 6 bits reduced to 4 by 1st-order modulator
- 6-bit signal subtracted from 4-bit signal gives 3-bit residual
- Both the 4-bit signal and the 3-bit signal are noise-shaped
- Gain errors between DACs result in shaped noise

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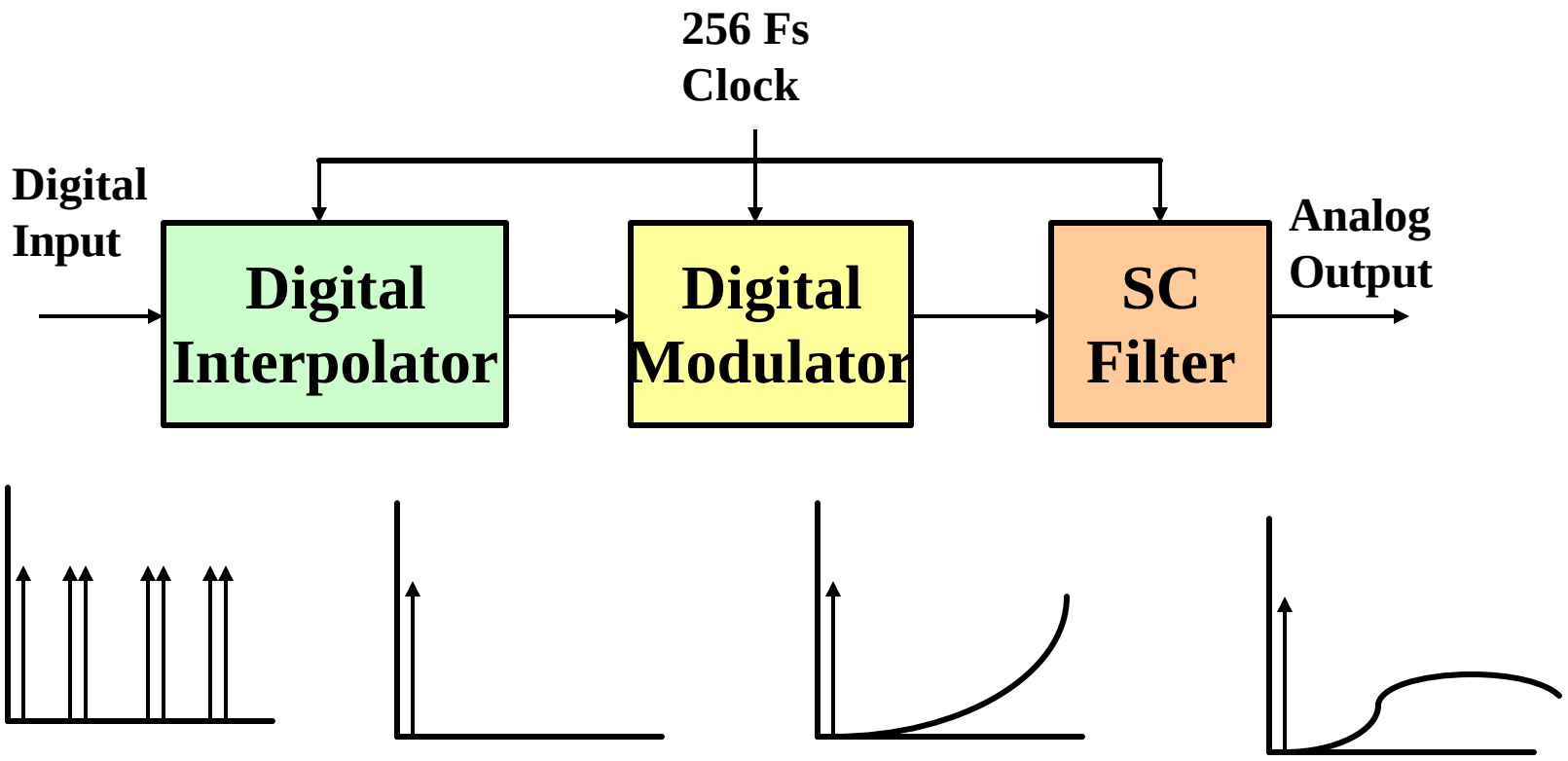
Conventional Discrete-time Sigma-Delta DAC

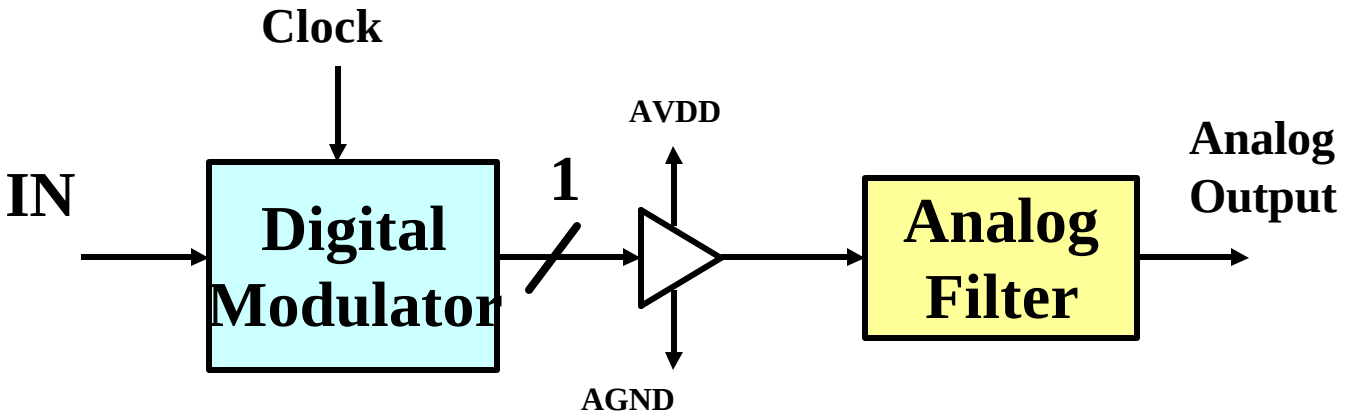


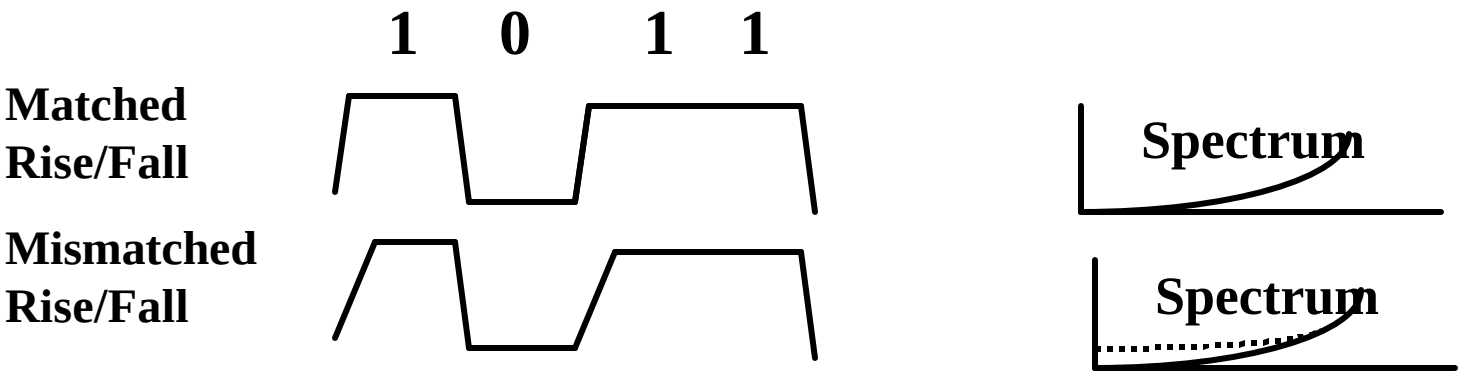
Problem: for very high SNR, SC filter is too big!

Solution:Continuous-Time Output Stage

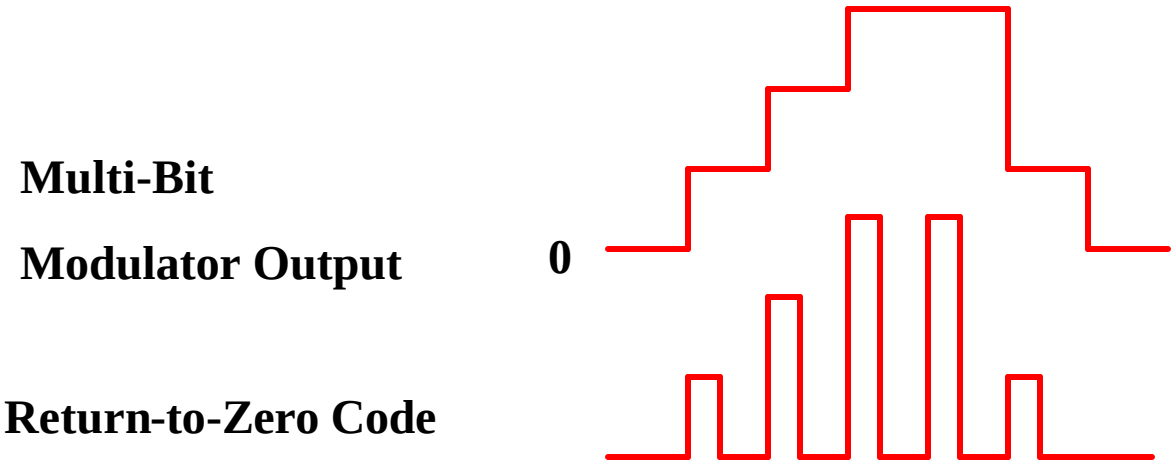
- Switched Capacitor Filter Approach
  - Capacitor size proportional to SNR^2
  - 110 dB performance = huge capacitors
- Continuous-time Output Stage Approach
  - Out-of-band noise reduced by multi-bit Sigma-Delta
  - analog matching – solved by scrambling
  - jitter sensitivity – solved by multi-bit approach
  - Final problem; Non-linear intersymbol interference.

Intersymbol Interference



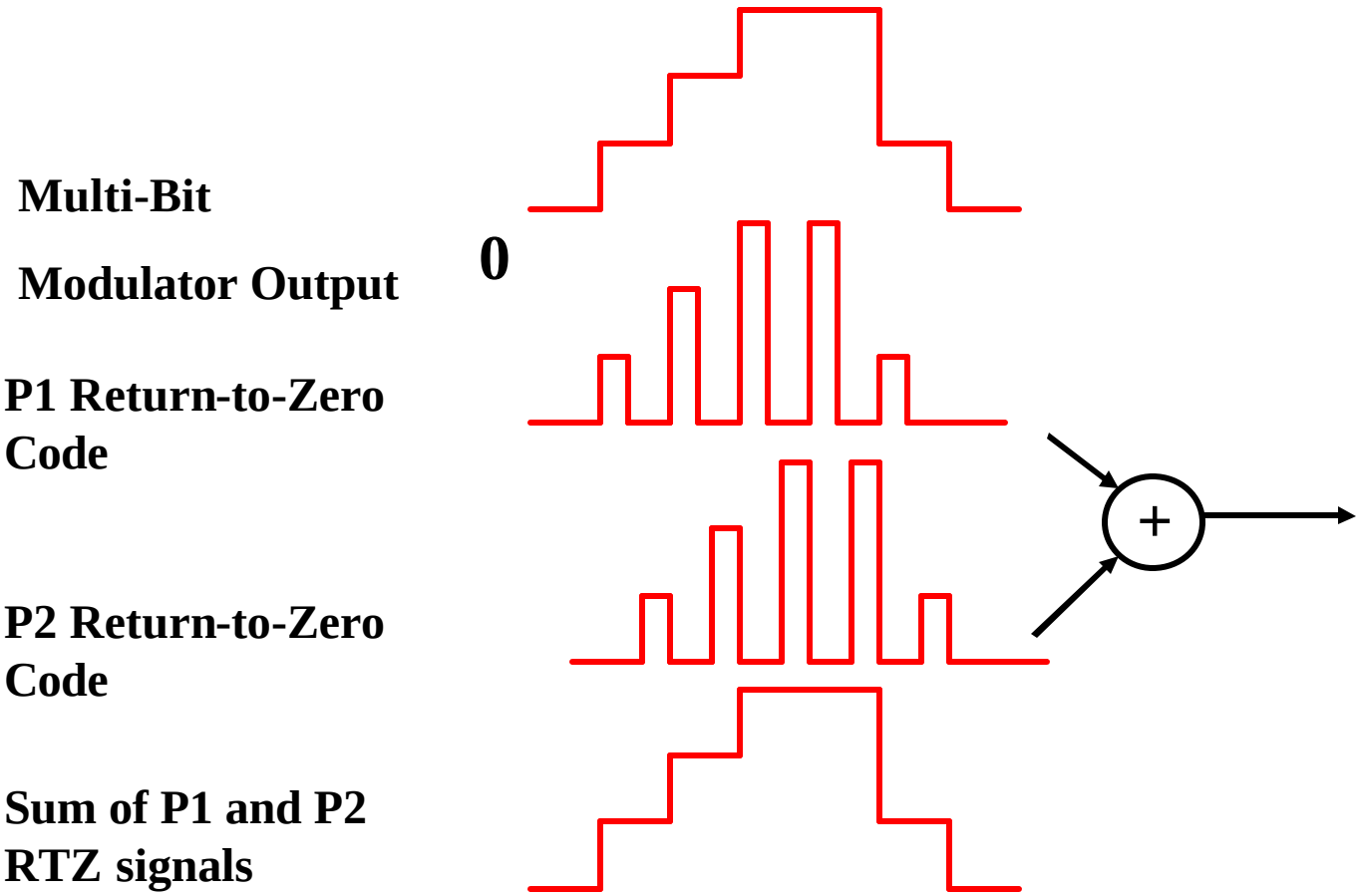


Return-to-Zero; a poor solution to ISI

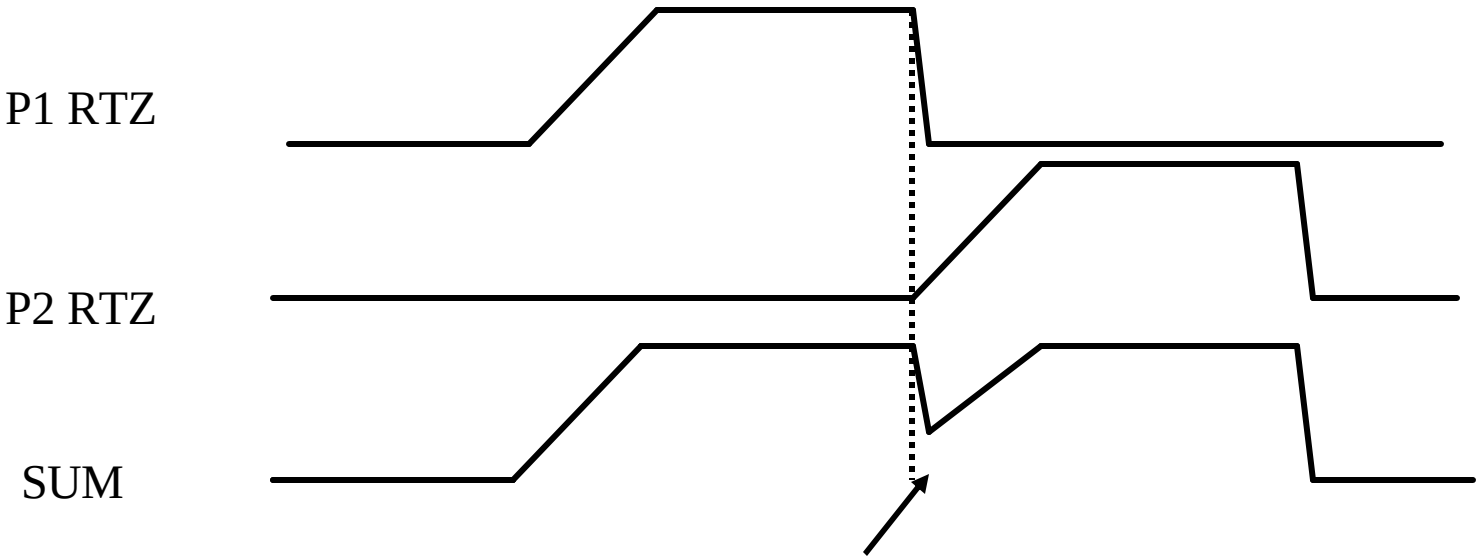


- **Return-to-Zero makes pulses ISI-free**
- **Large voltage steps cause extreme jitter sensitivity**
- **Large steps cause problems for the analog lowpass filter**
- **Output range (after filtering) reduced by a factor of 2**

Dual Return-to-Zero

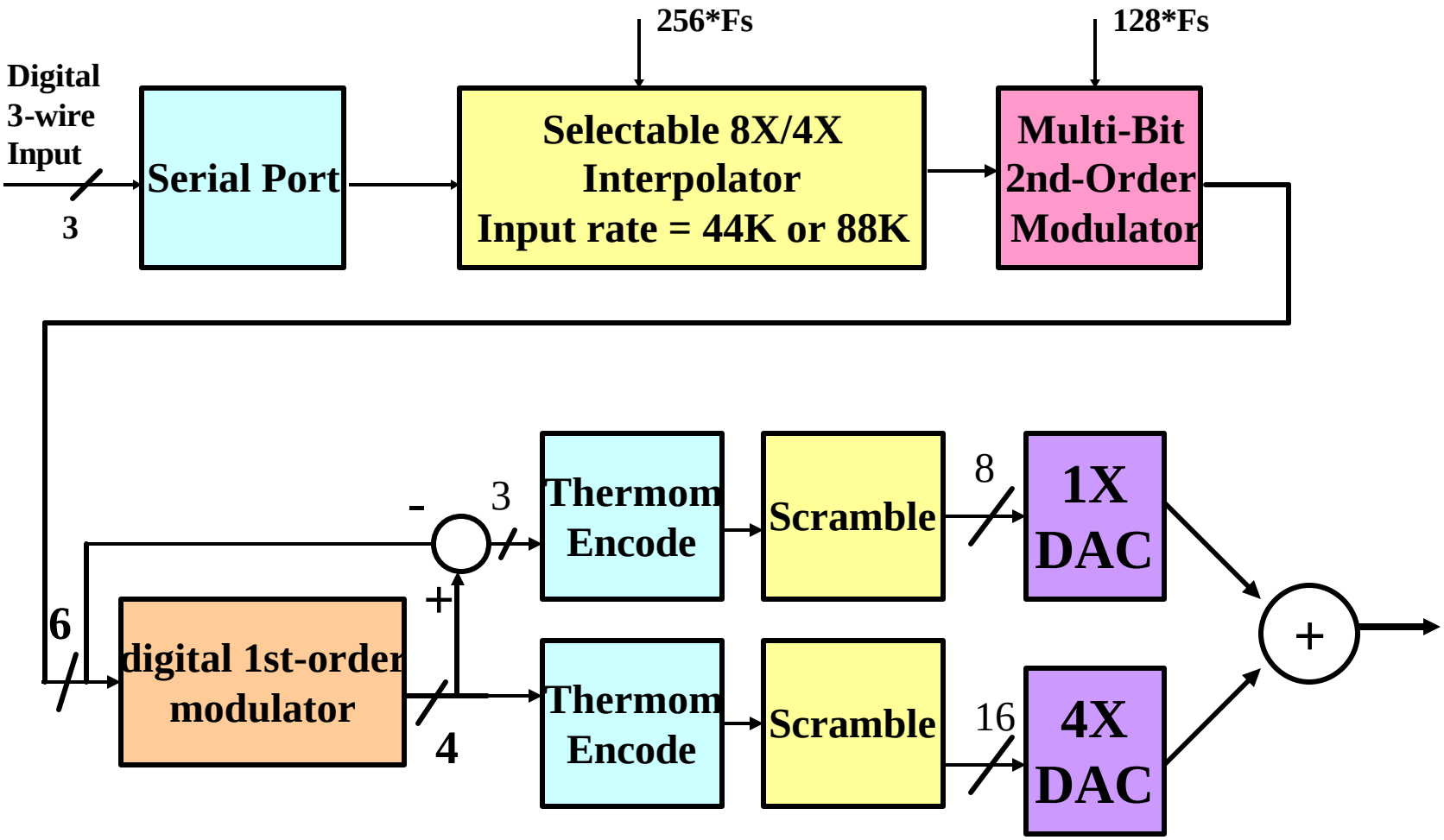


Time-domain explanation of Dual Return-to-Zero

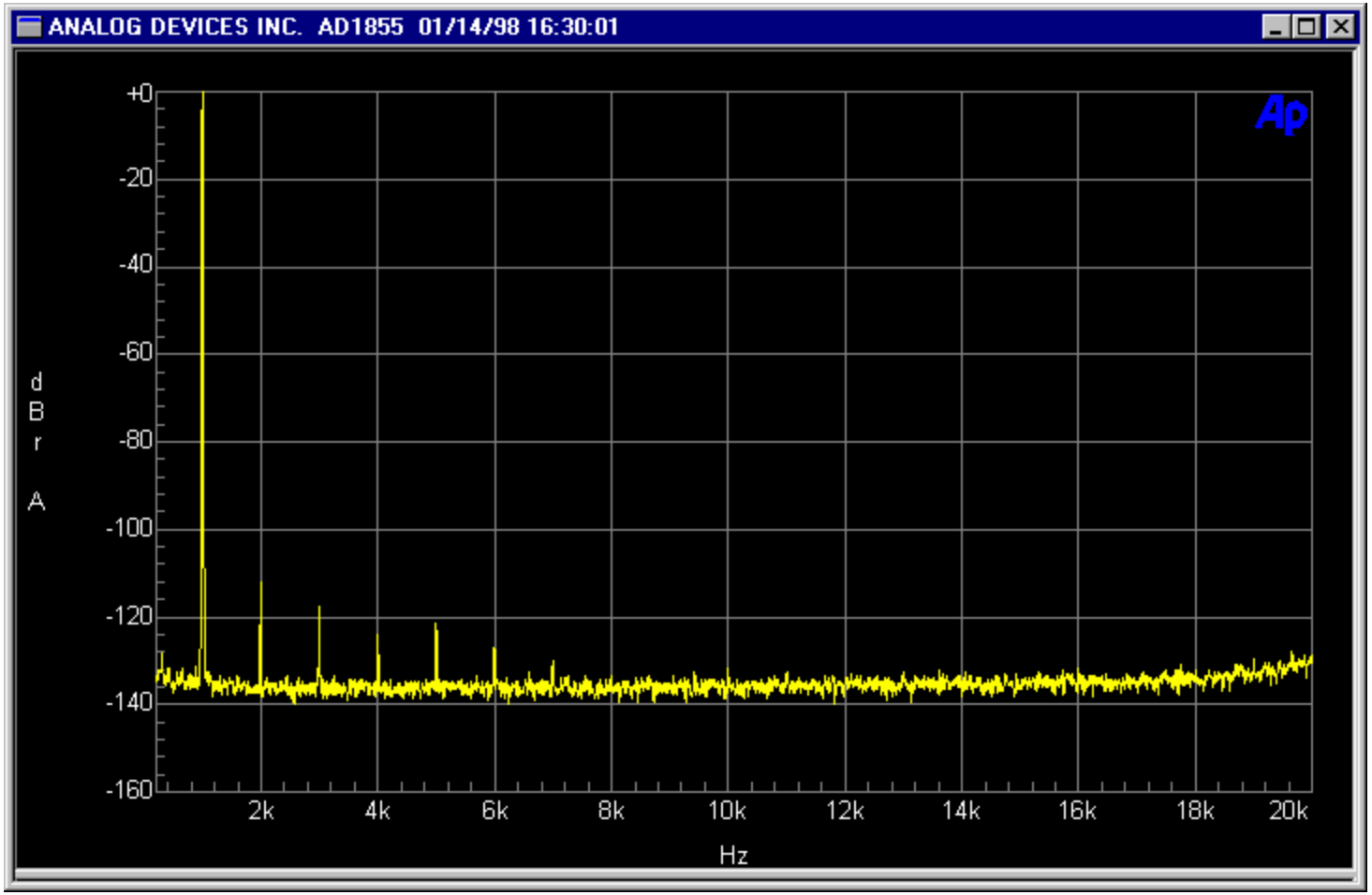


- Rise/Fall mismatch causes “glitch” in summed waveform
- This “glitch” causes the area under the sum waveform to be independent of the previous bit decision.

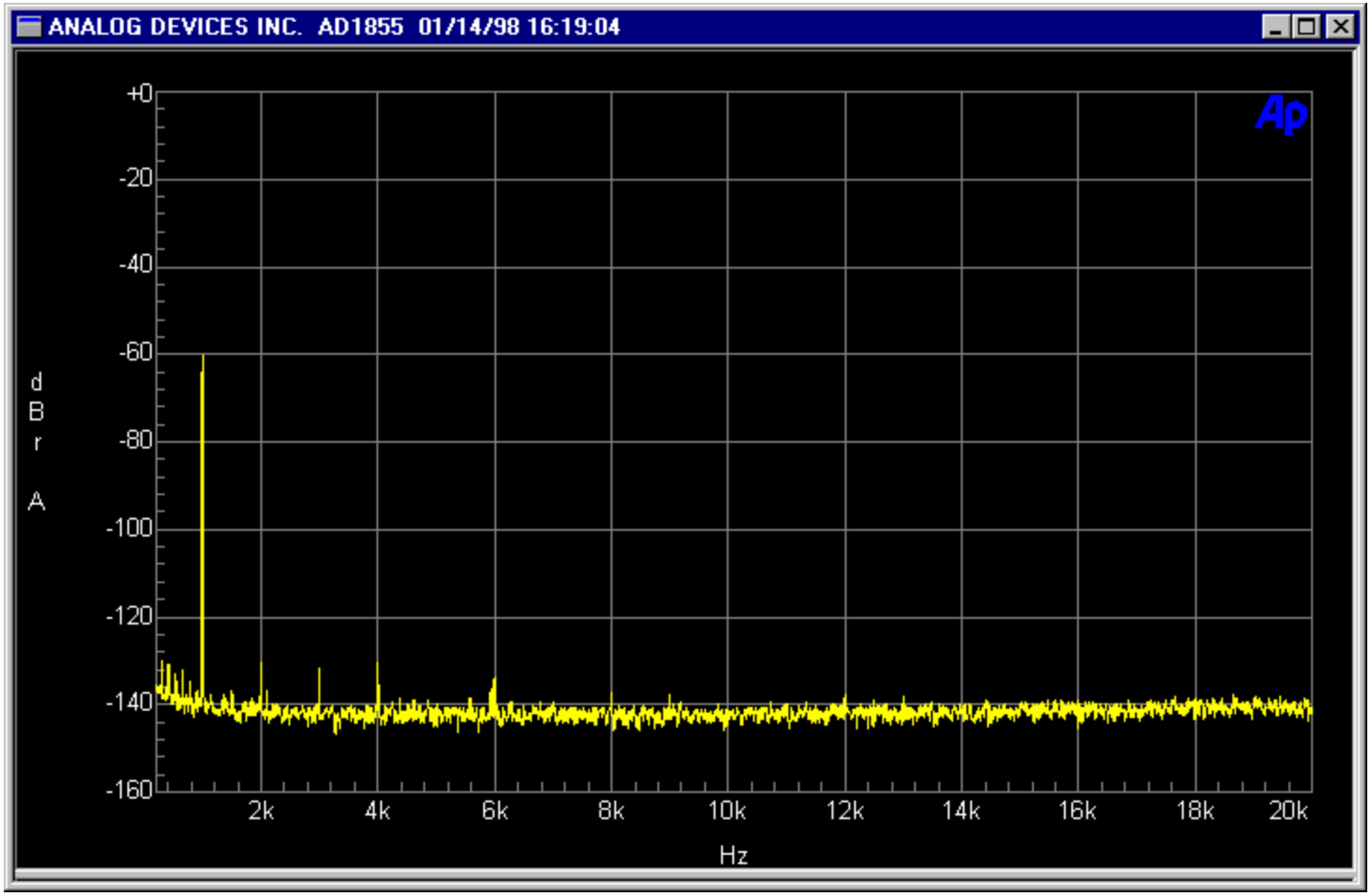
Typical Chip Implementation (1 channel of 2)

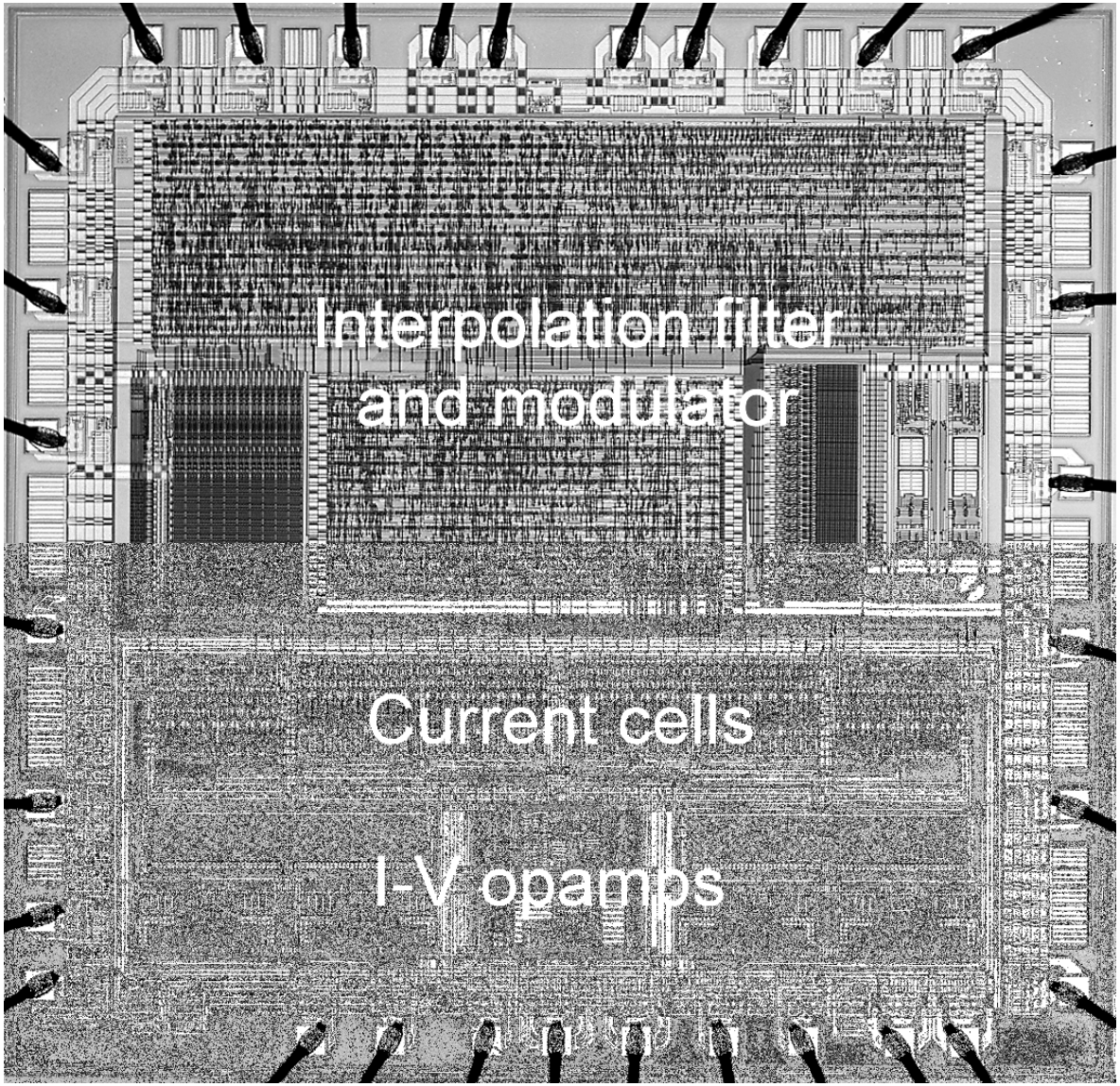


FFT with Full-Scale 1KHz Input (8K Points)



FFT with -60 dB Input (8K Points)




Interpolation filter
and modulator
Current cells
I-V opamps

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What's wrong with discrete-time processing (switched-cap)?

- For HIGH-PERFORMACE converters, the capacitor sizes become very large (doubles for every 3dB of SNR.)
  - Hard to drive these caps (both internal and external)
  - Large chip area
- For ALL designs with large digital content;
  - Small glitches that occur at the sampling instant get trapped.
  - Not always possible for the digital section to have a "quiet spot" for clean sampling. Digital clock rates have become too high.

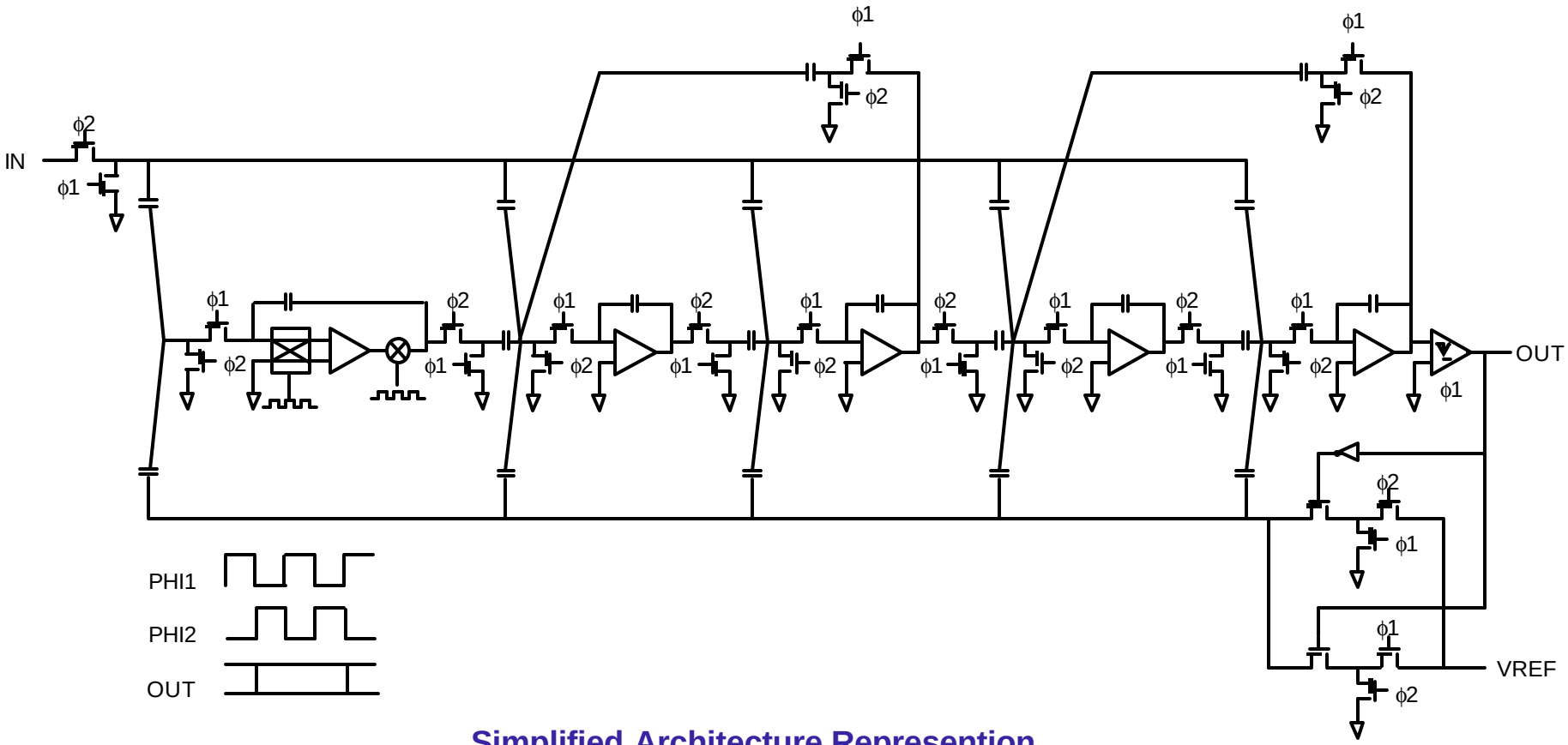
Continuous-time Advantages

- High SNR means small resistors, not large capacitors
- Digital glitches are not sampled; high-performance converters + massive digital processing is possible.
- Easy to debug
- Better chance of 1st-silicon success

Continuous-time Disadvantages

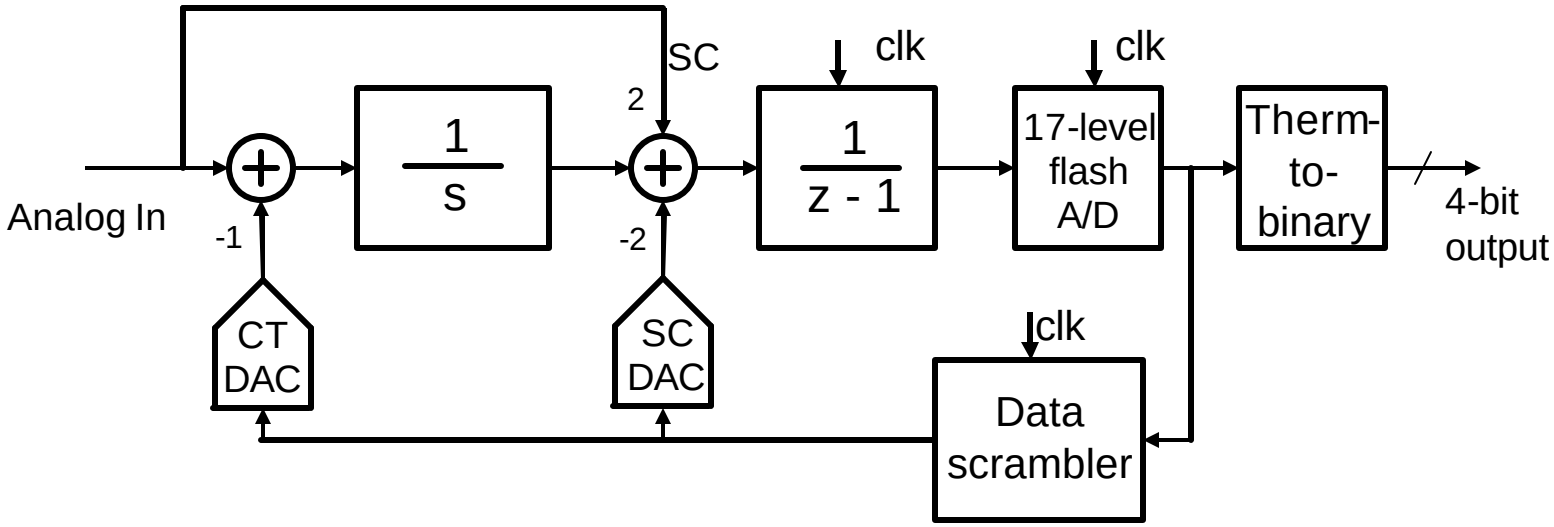
- Jitter sensitivity
  - Can be cured by using multibit DACs
- Multi-bit DACs have distortion with imperfect matching
  - Can be cured by using scrambling
- R-C time constant does not track with sample-rate (problem for ADC only)
  - Must use some ratio tracking mechanism
- Large time constants require either off-chip components or large on-chip capacitors.
  - Use continuous-time in first-stage only, other stages may be built using switched-cap (for ADCs).

5th Order ΣΔ ADC, circa 1990



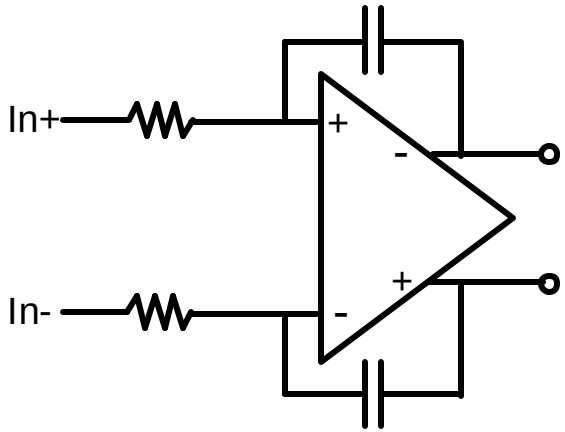
Simplified Architecture Represention

ΣΔ modulator with CT+DT Loop Filter, 2005

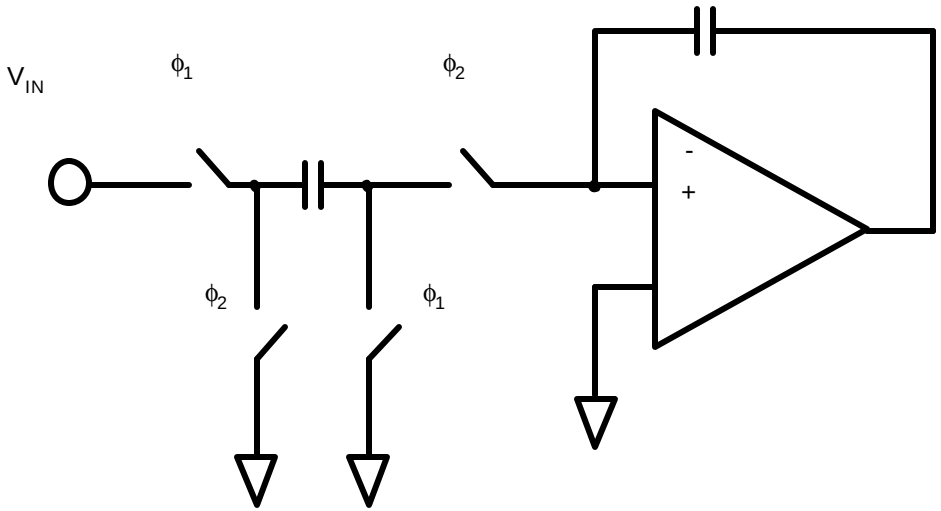


- OSR = 128
- Multi-bit quantization allows reduction of loop order to 2
- Theoretical SNR ~ 117dB

Integrator designs



Continuous-time differential

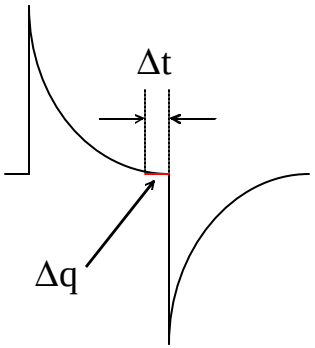


Discrete-time single-ended

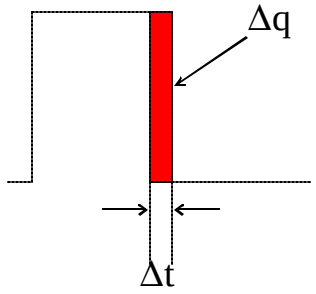
Clock Jitter

How does this affect the Dynamic Range?
Time domain view

Switched-capacitor
charge delivery

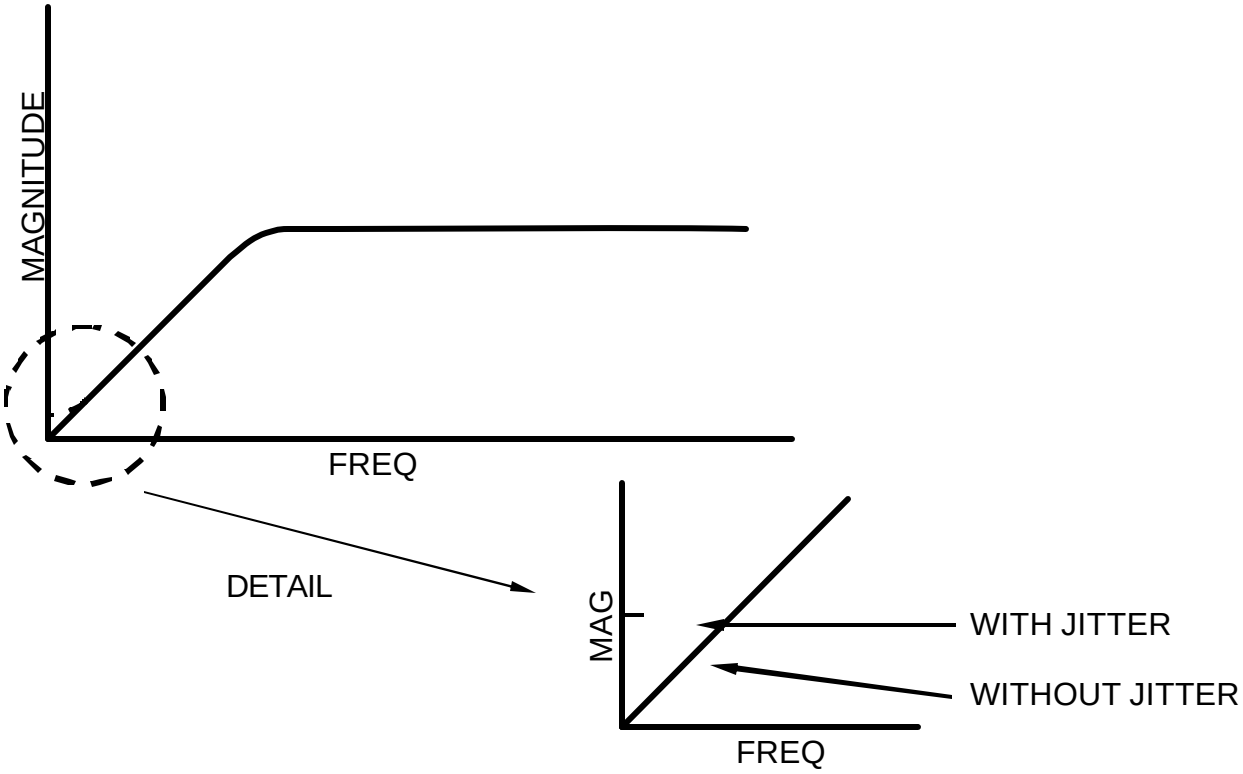


Continuous-time
charge delivery



Clock Jitter

Clock jitter adds random phase modulation to the output bit stream. This causes the high-frequency noise to fold down to the audio band, raising the converter noise floor.



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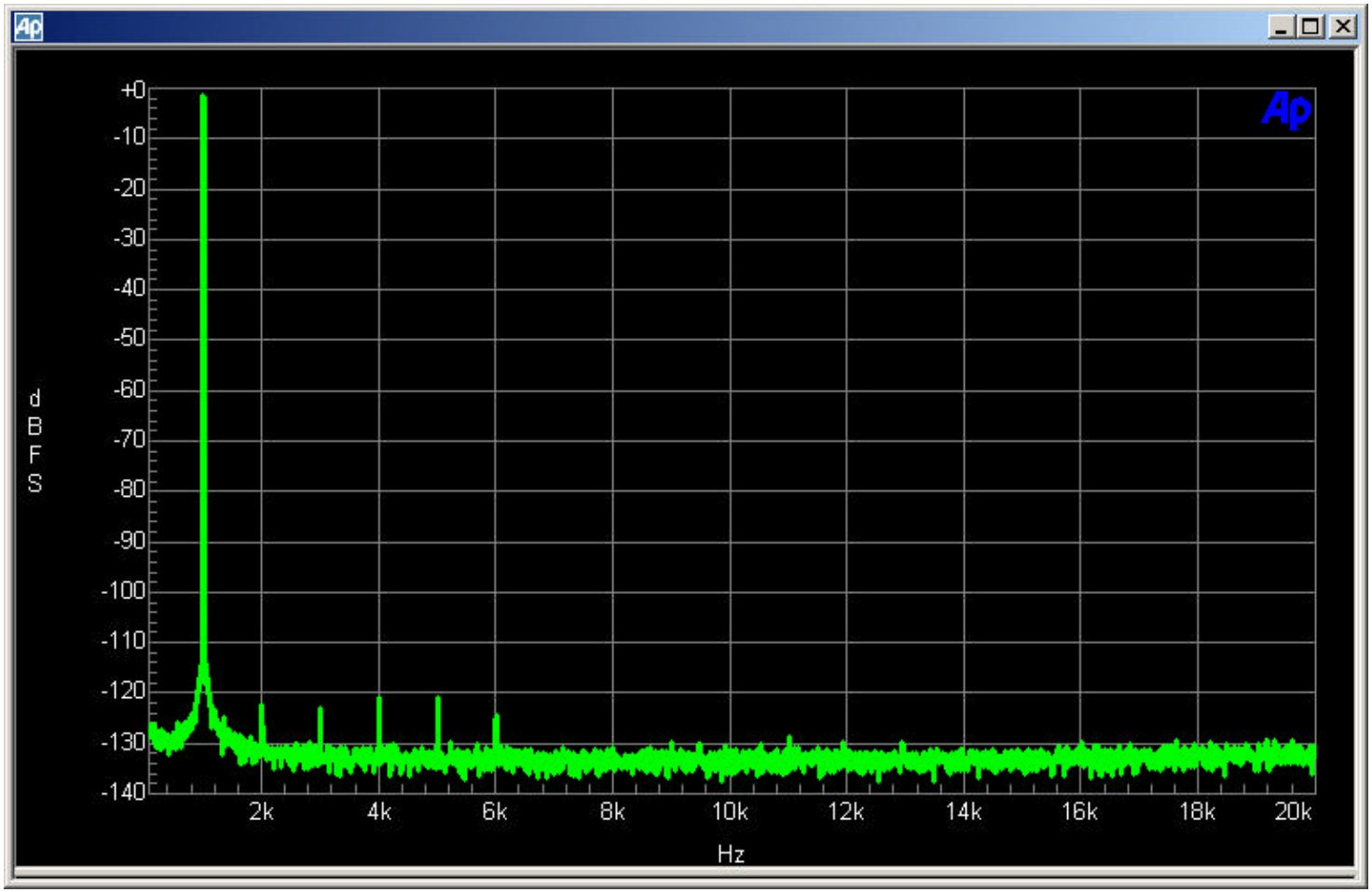
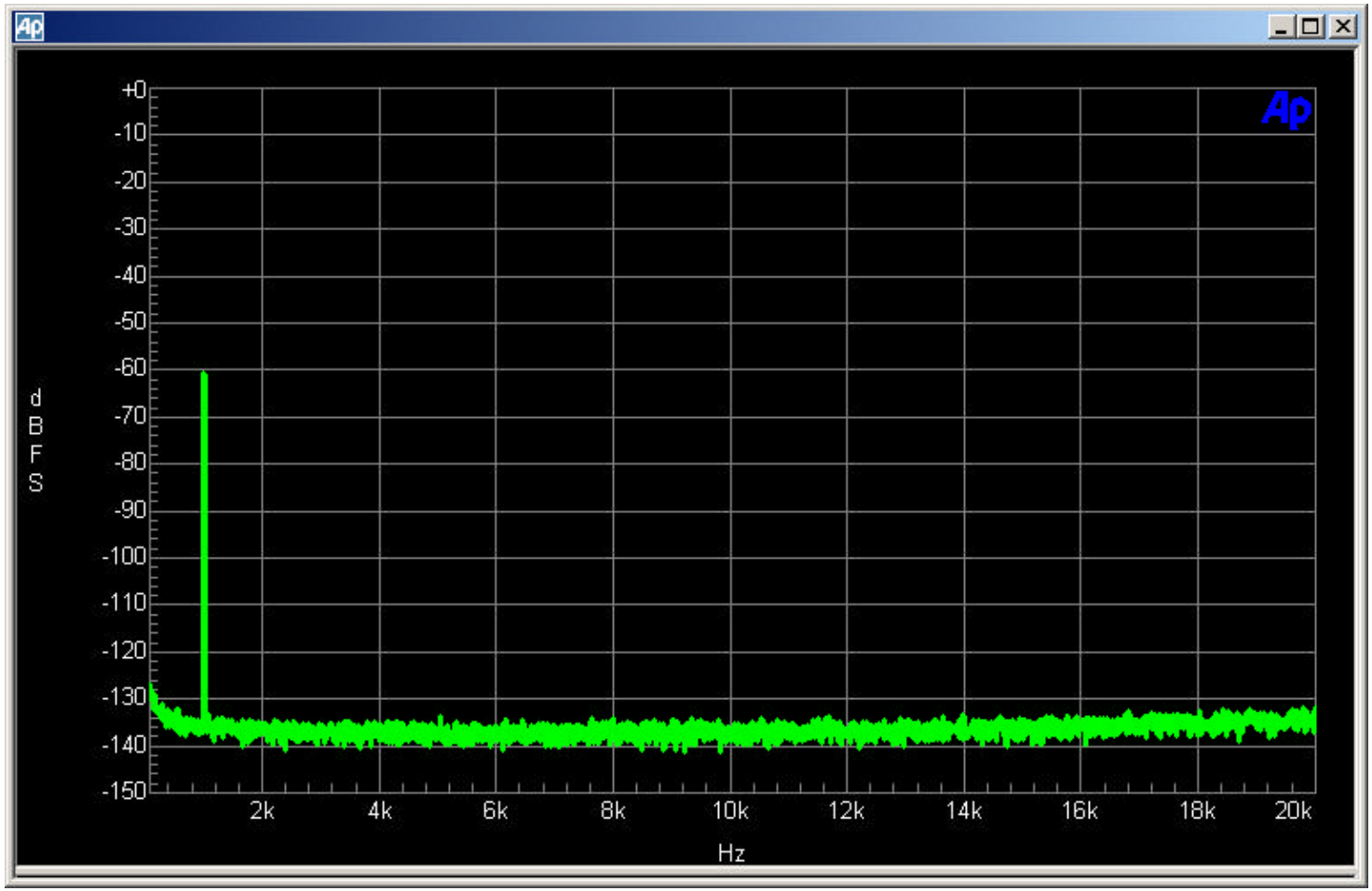
- New architectures – from 1 bit to Multi-bit
  - Multi-bit Mismatch Shaping
  - Split Noise-shaping
- New Architectures; Continuous-time and mixed cont/discrete loops
  - CT DACs
  - Overcoming Intersymbol interference
  - Performance
  - Mixed CT/DT ADCs
  - *Performance*
- New Architectures; Power Sigma-Delta (“class-D” amplifiers)
- New architectures; misc
  - Bandpass sigma-delta
  - Complex sigma-delta
- Research work
  - Array sigma-delta
  - The Grand Unified Theory of Everything; Inverted-FIR sigma-delta

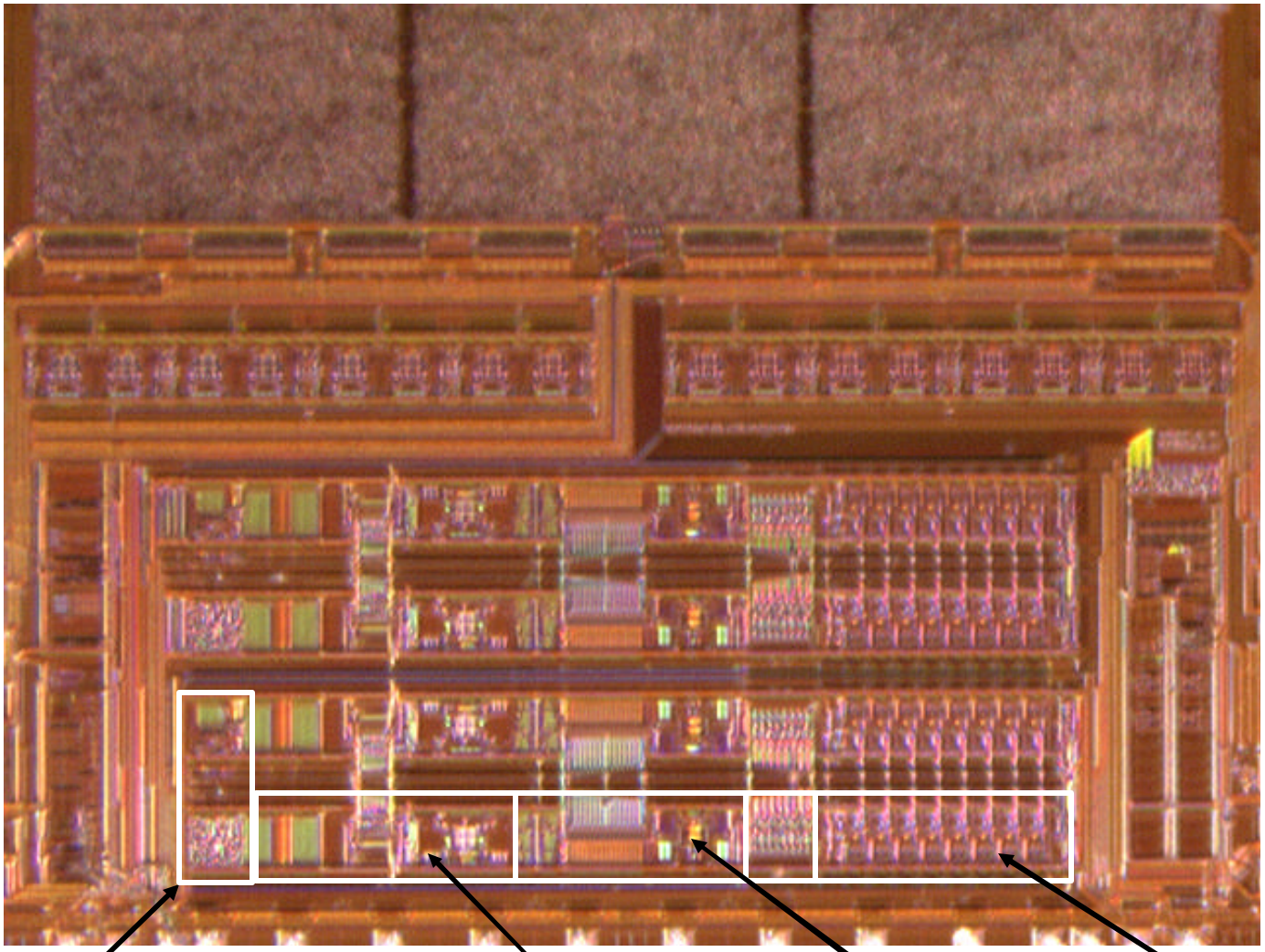
8k FFT Plot of -1dBFS, 1kHz tone, AD1838



8k FFT Plot of -60dBFS, 1kHz tone



Chip Photograph



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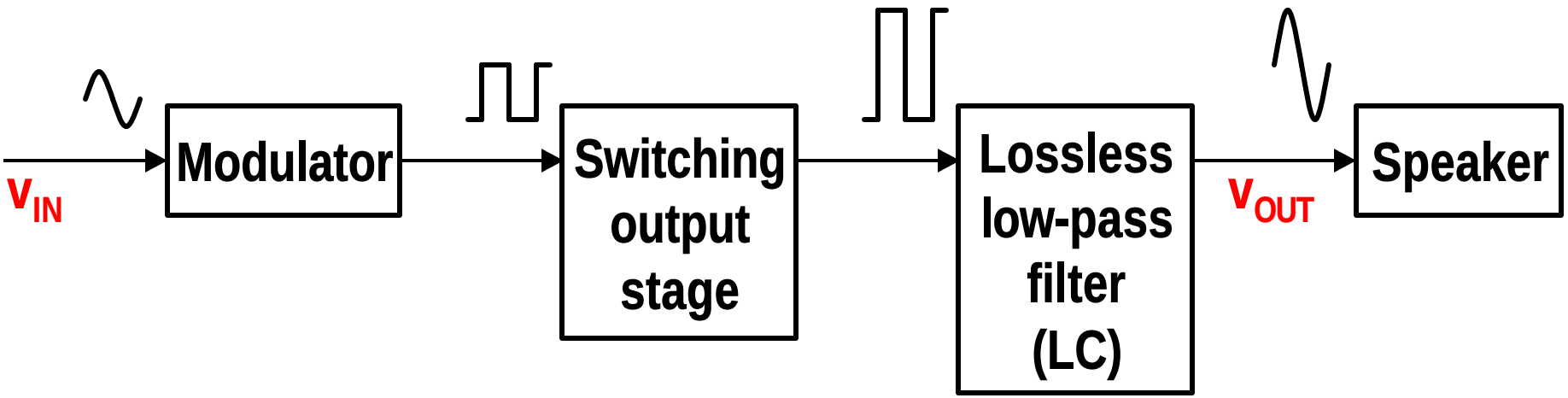
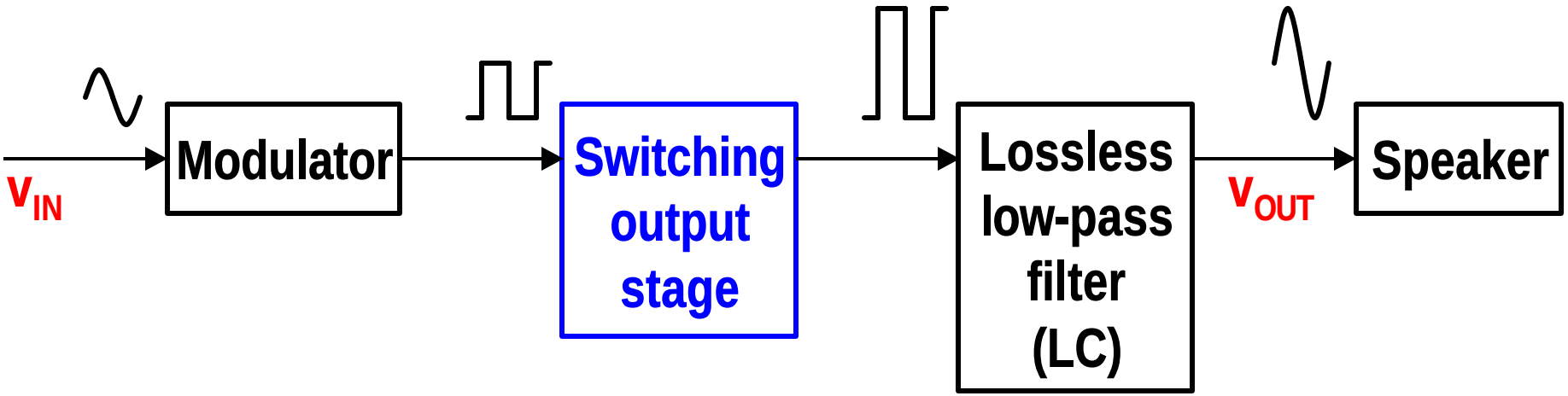
Introduction: Generic class D amplifier diagram

- A ‘class D’ amplifier has several elements:



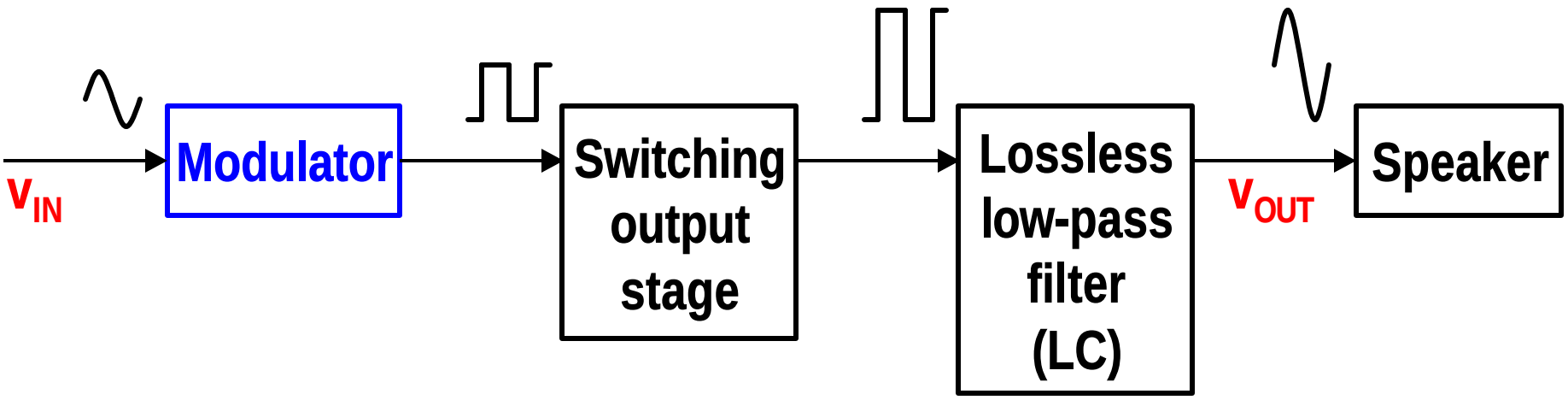
Introduction: Generic class D amplifier diagram

- The switching output stage is the defining element:
  - it outputs pulses that switch between + and – supplies.
  - This waveform allows high power efficiency, because v across output device is small when it conducts i, giving minimal power dissipation v*i.



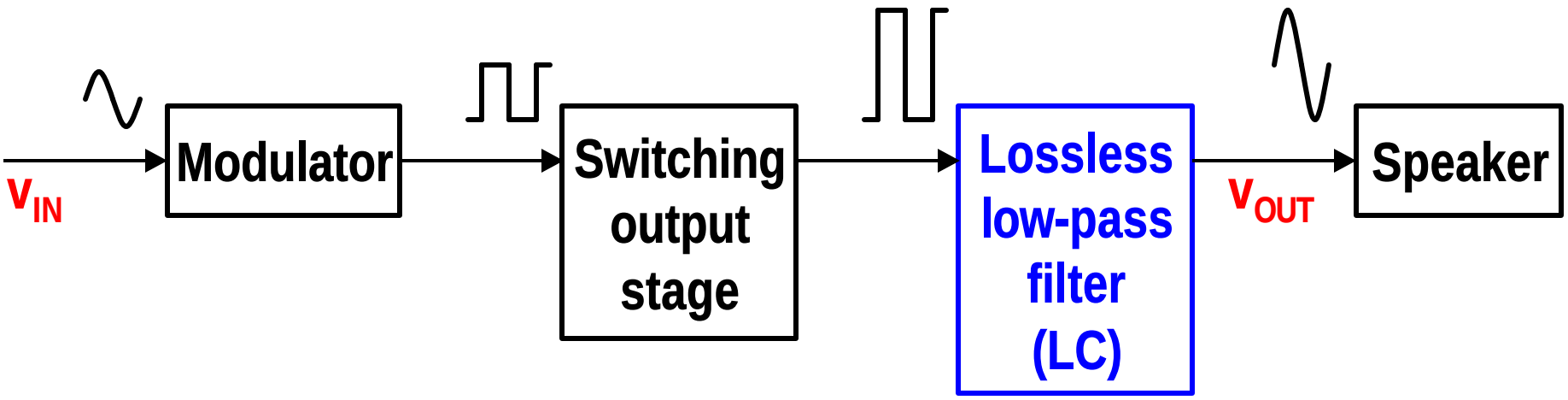
Introduction: Generic class D amplifier diagram

- Most audio signals are not pulse trains, so to use a switching output stage in an audio amplifier, we also need a modulator, to convert input audio into pulses.

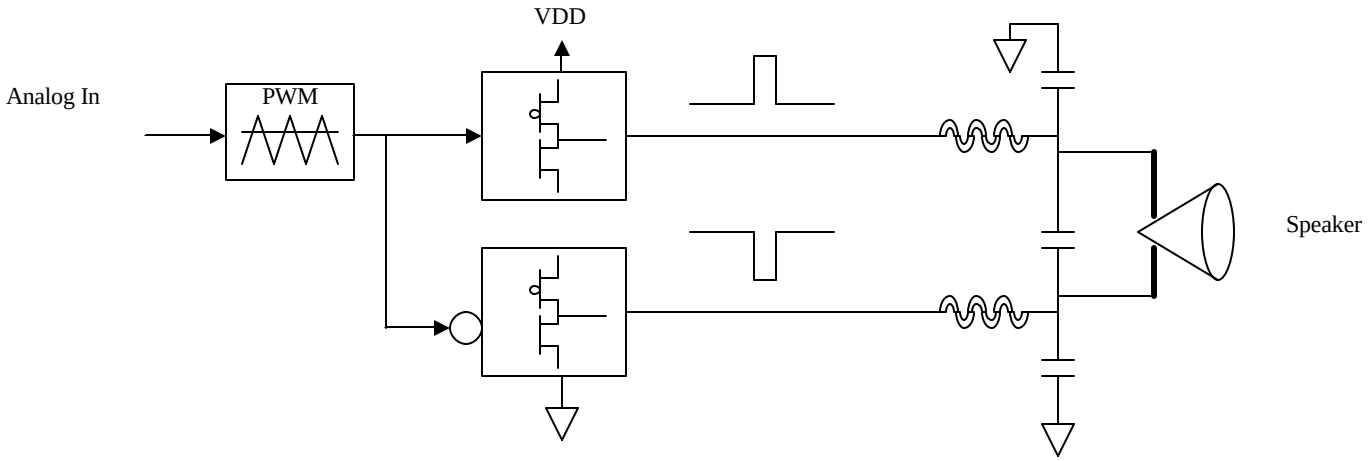


Introduction: Generic class D amplifier diagram

- A low-pass filter is often used downstream of the output stage, to attenuate undesirable high-frequency components of the output stage pulses.
  - Must be lossless to preserve efficiency benefit!
  - Passive, LC filter is usually used



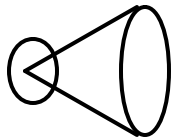
Traditional Analog PWM Modulation



- Switching rates are commonly between 200KHz and 500KHz.
- Efficiency can be high (> 85%)
- Problems; EMI, open-loop output stage (distortion), no PSRR

Basic 2-state Analog PWM

Half-Bridge 1

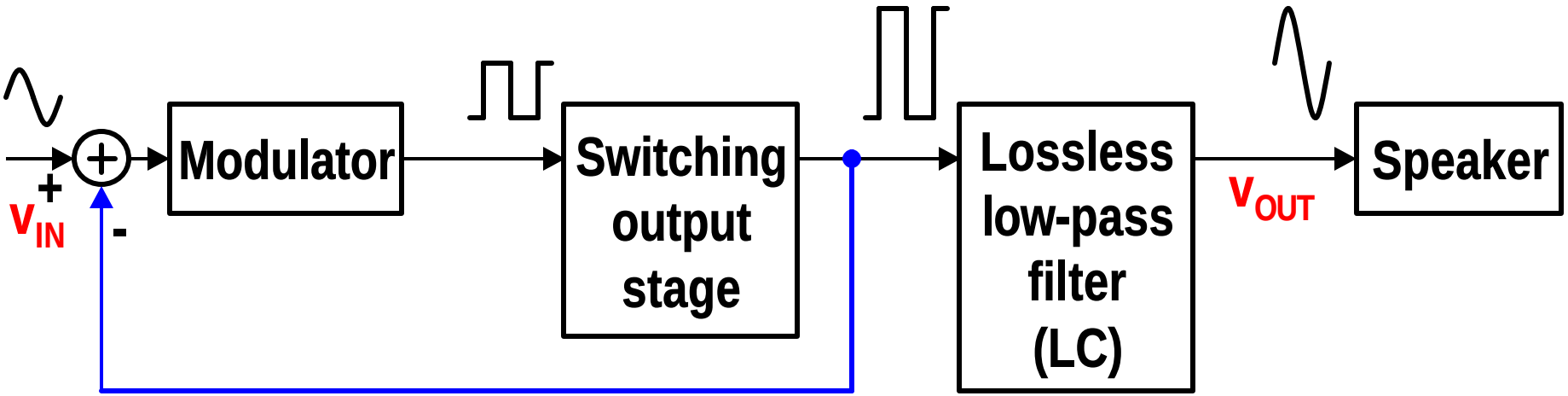


Half-Bridge 2

Input

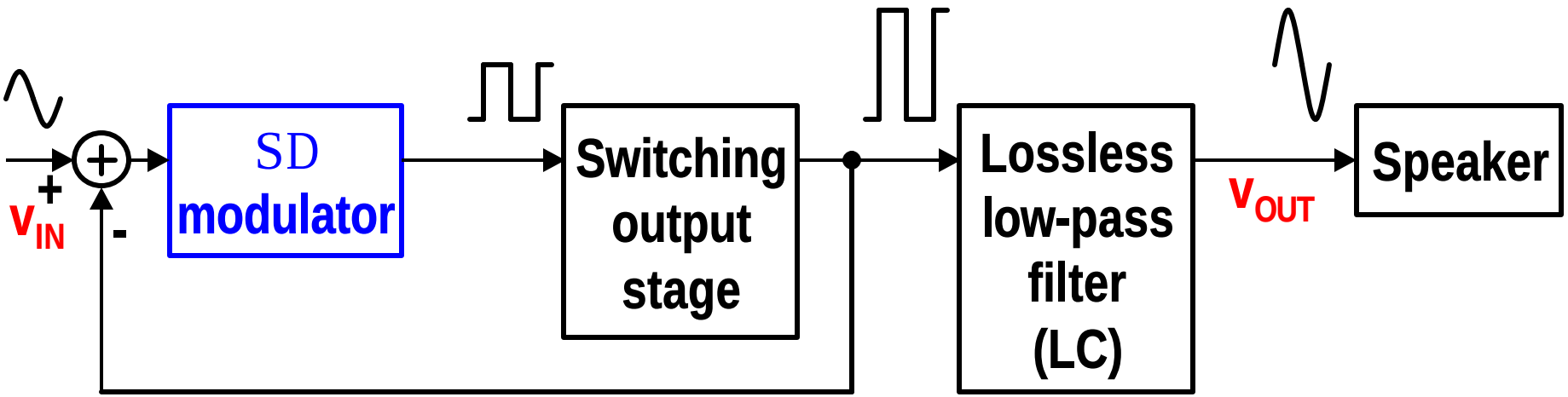
Introduction: Class D amplifier special features

- Feedback from output stage → modulator
  - Corrects power stage non-idealities:
    - non-overlap time,
    - voltage overshoot/ringing,
    - nonzero rise and fall times.
    - unmatched, nonlinear rising and falling edges.
  - Provides PSRR, for output stage power supply



Introduction: Class D amplifier special features

- 1-bit ΣΔ modulator (instead of PWM)
  - + Less distorted output than PWM modulator
  - + Fewer high-energy, high-frequency peaks in output spectrum than PWM (no PWM clock harmonics to worry about)

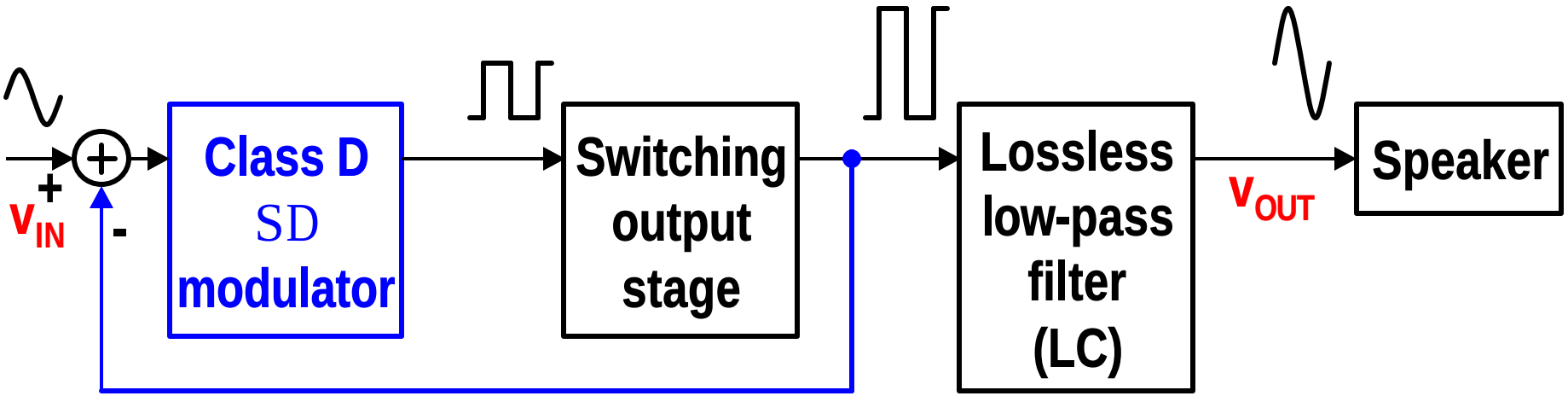


Introduction: Class D amplifier special features

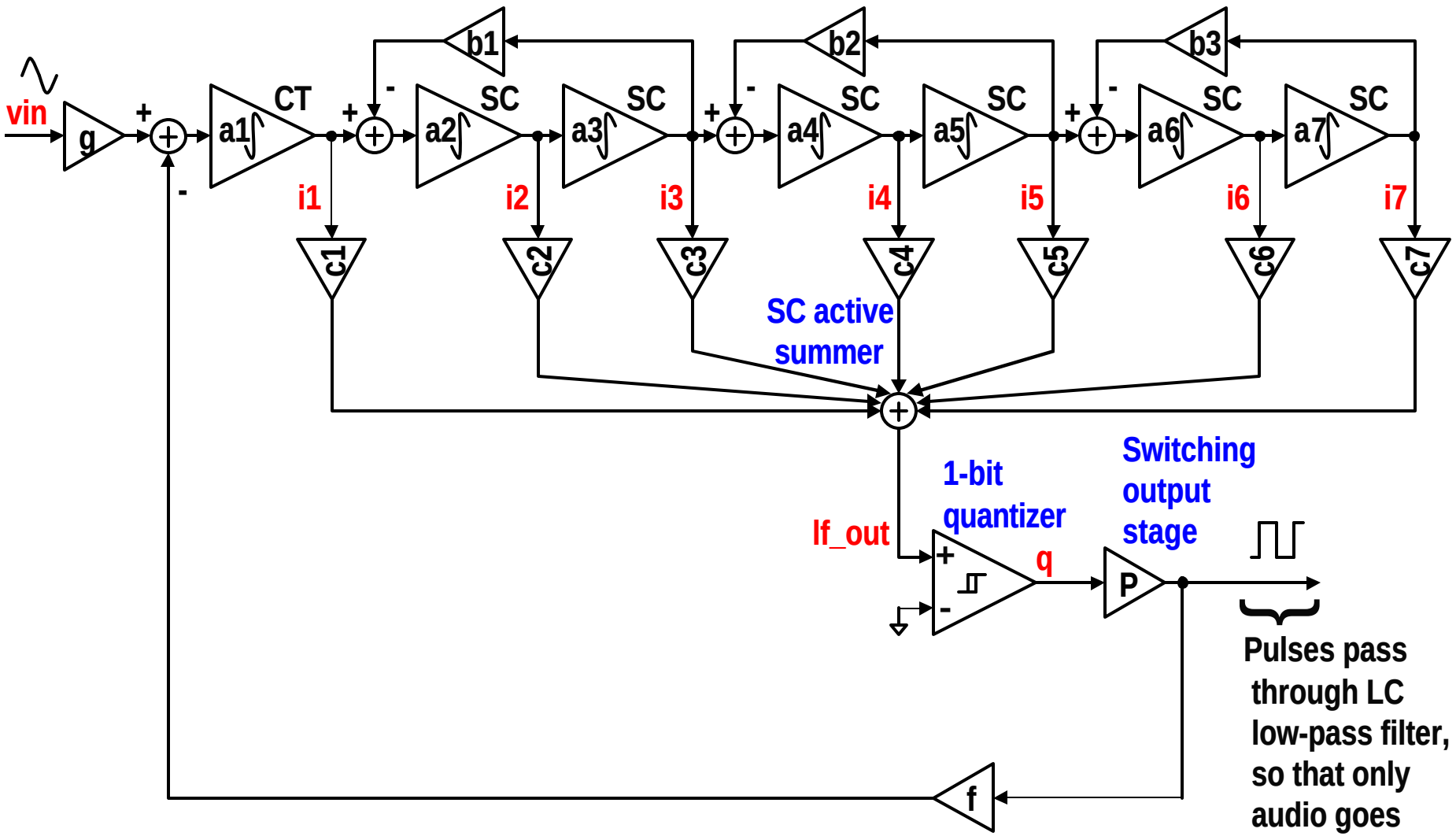
- A conventional 1-bit ΣΔ modulator has several significant drawbacks!
  - Stability limit near 0.5 limits max output power to 0.5^2 = 0.25 x theoretical full-scale (tiny!)
  - For typical audio OSRs, ΣΔ output bit rate is 1MHz – 2MHz
    - (much higher than typical PWM clock of 400kHz)
    - gives increased switching losses
- For these reasons, conventional ΣΔ modulators are rarely used in class D amplifiers.....

Introduction: Class D amplifier special features

- Overcoming the obstacles
  - Improved stability limit from 0.5 to 0.9:
    - conventional 0.5 ‘limit’ arises from optimizing in-band SNR:
    - Can instead trade off stability for suboptimal noise-shaping
    - Our modulator is 7th order with ‘only’ 112dB audio-band SNR, but is stable up to 0.9.
  - Reduced output bit rate to ~500kHz with ‘dynamic quantizer hysteresis’
    - (More on this later)



Modulator: (architecture, hysteresis not shown)



Definition of “Hysteresis”

Assume OUT can take on values of +/- 1

Comparator equation with no hysteresis;

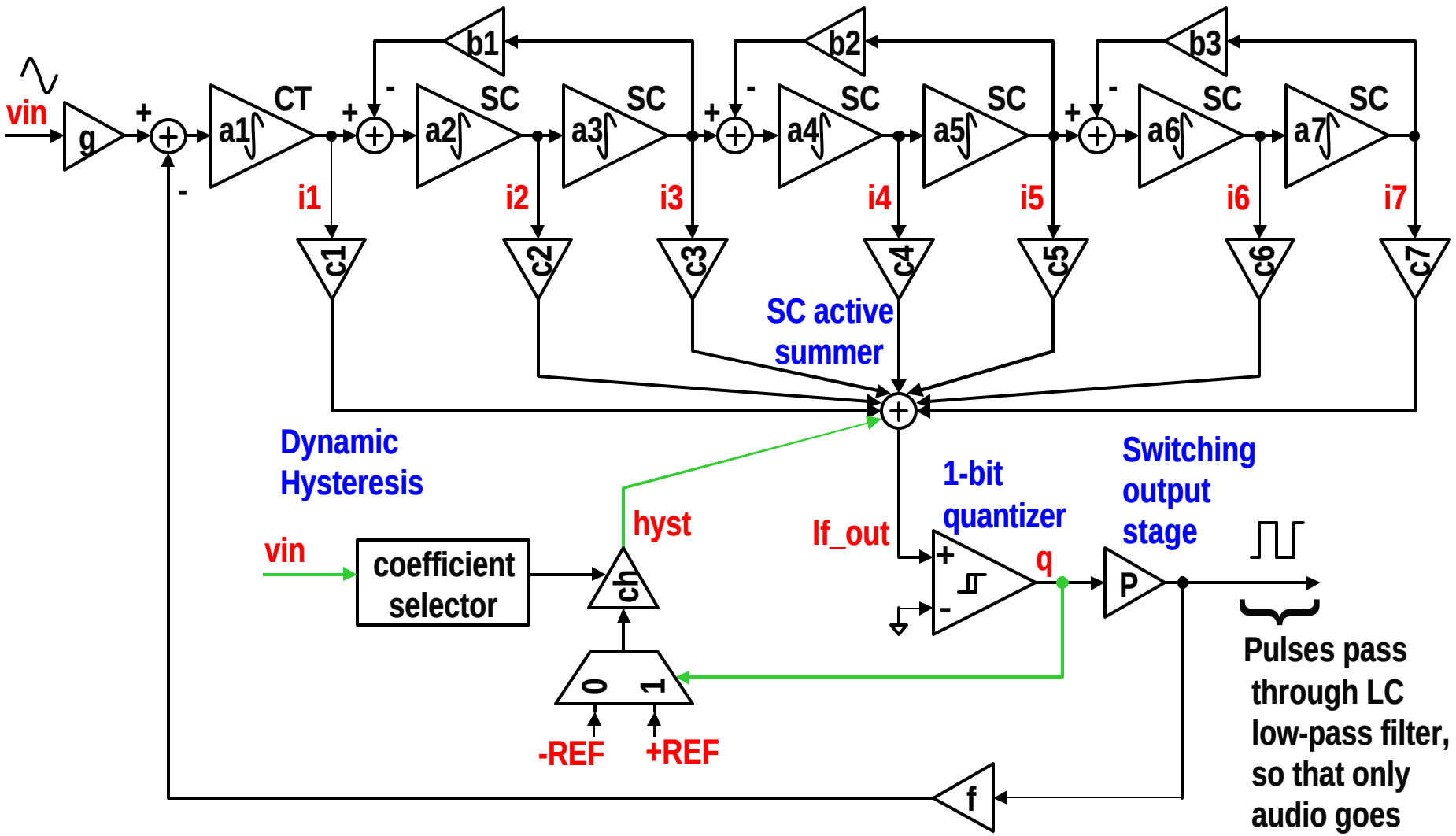
if(IN > 0) OUT = +1.0; else OUT = -1.0

Comparator equation WITH hysteresis;

Threshold = -OUT*k, k is the “hysteresis factor”, usually < 1

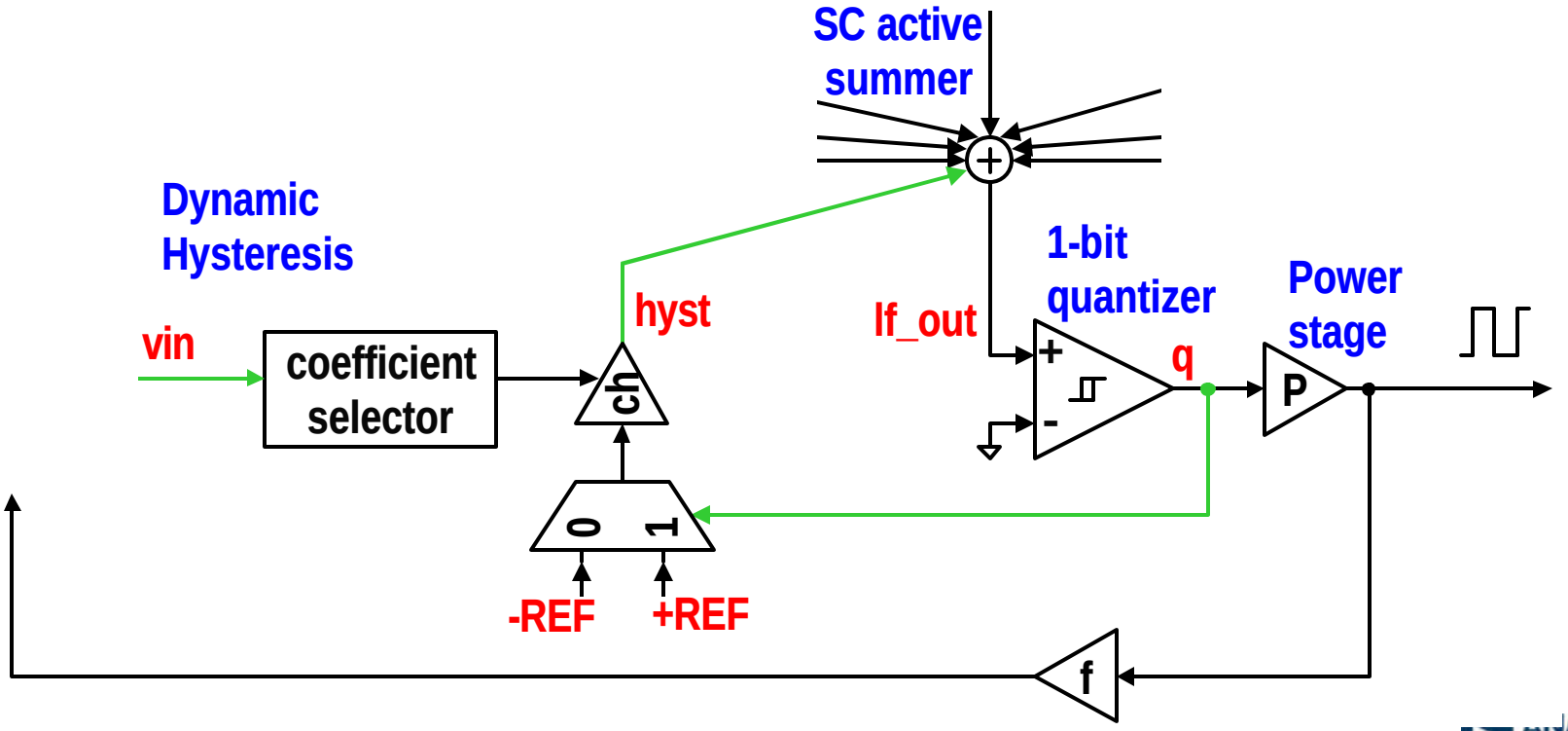
if(IN > Threshold) OUT = 1.0; else OUT = -1.0

Modulator: (architecture, including hysteresis)



Modulator: (Dynamic quantizer hysteresis)

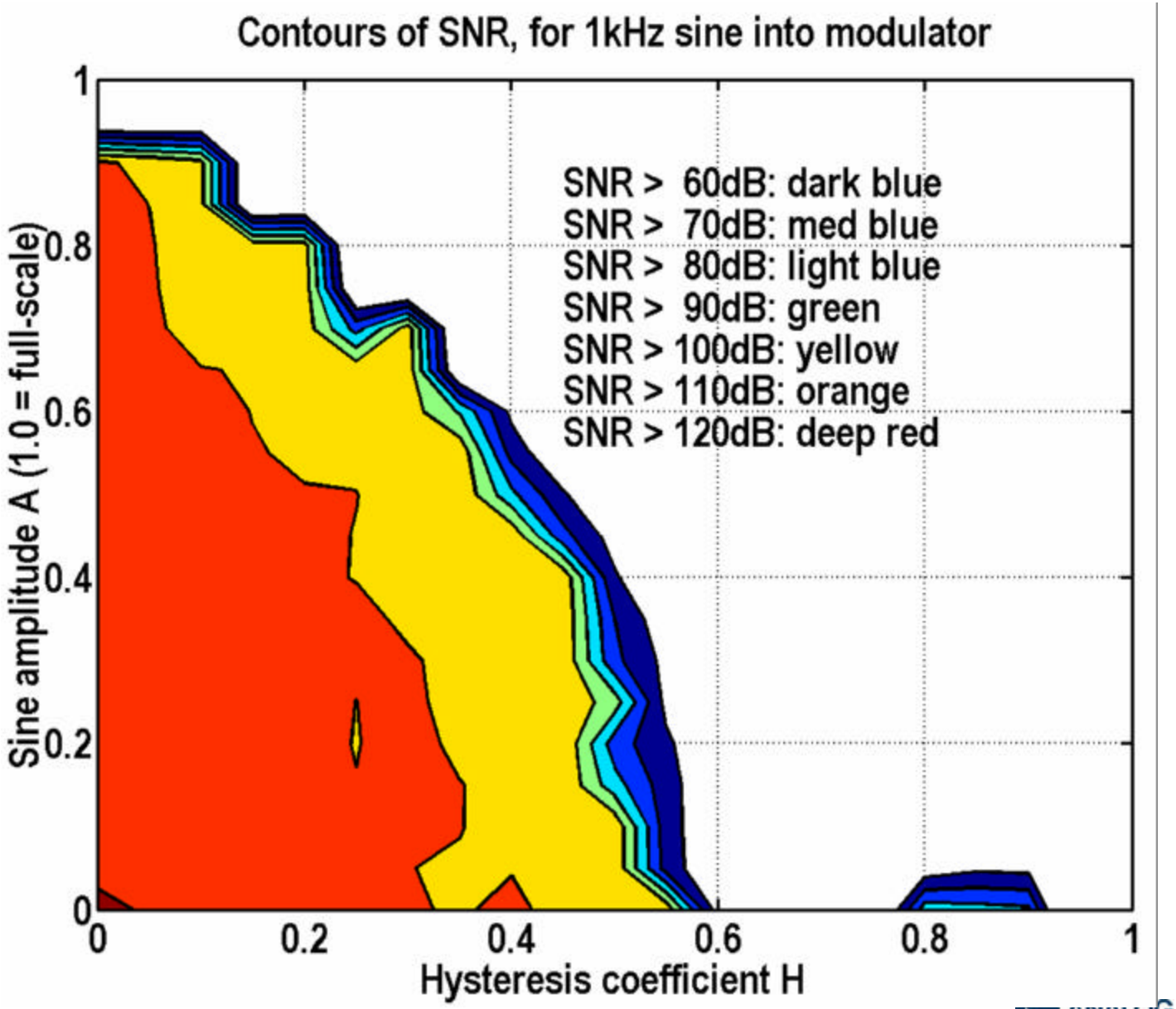
- Adding hysteresis amount H to quantizer reduces q's transition rate, because integrators must now integrate until lf_out crosses +/-H (instead of 0).



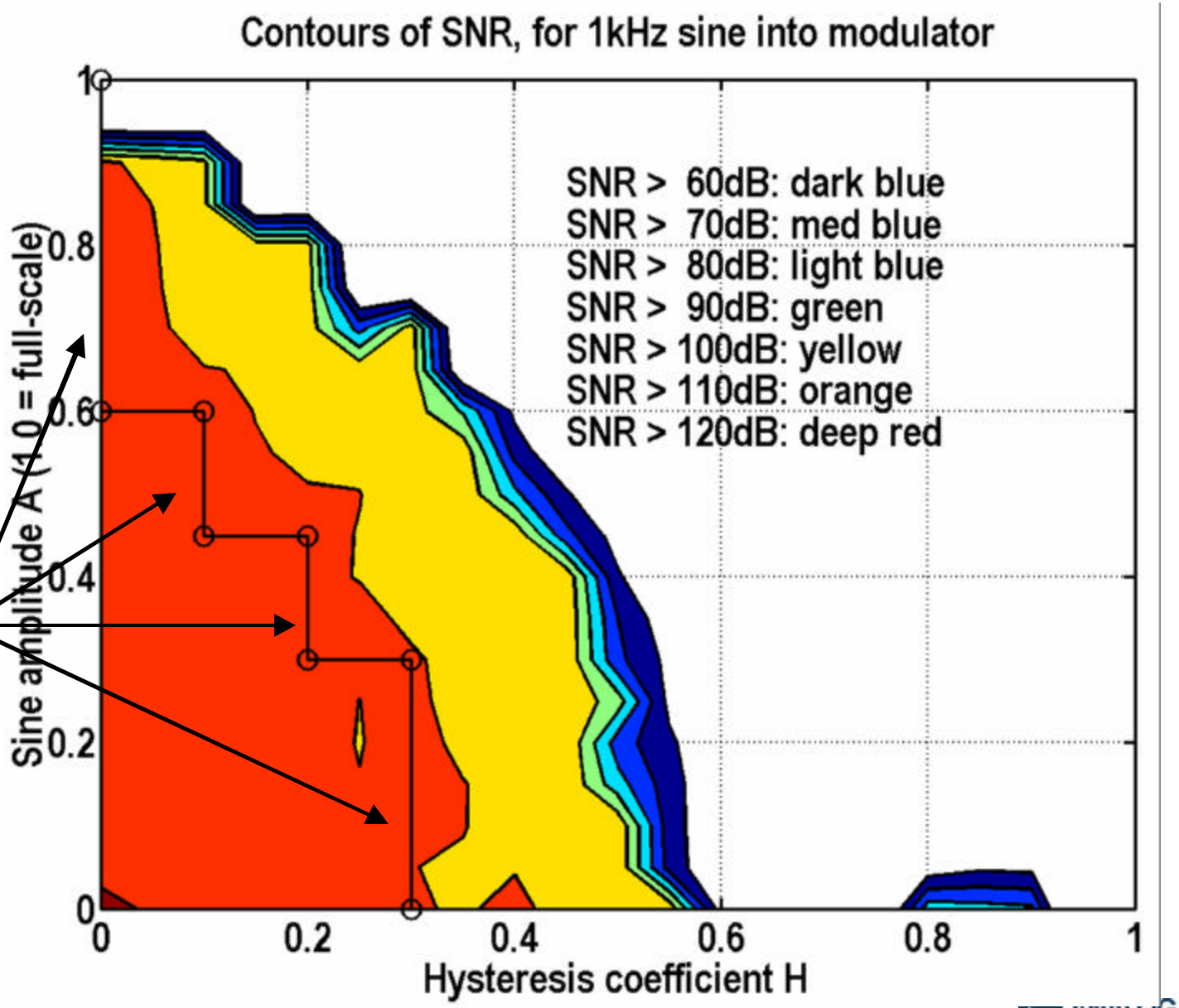
Modulator: (Dynamic quantizer hysteresis)

- But quantizer hysteresis H degrades modulator stability. (i.e. stability ↓ as H ↑)
  - (Problem at high input levels, since stability also ↓ as v_{IN} ↑)
- So H that's safe for low v_{IN} may be unsafe for higher v_{IN}.
- No single H can significantly reduce bit rate AND keep the modulator stable, for all signal conditions!
- Try adjusting H DYNAMICALLY:
  - Monitor v_{IN}, choosing large H for small v_{IN}, but small H for large v_{IN}, thus maintaining modulator stability over all signal conditions, while maximally reducing the modulator bit rate.

Modulator: (Dynamic quantizer hysteresis)



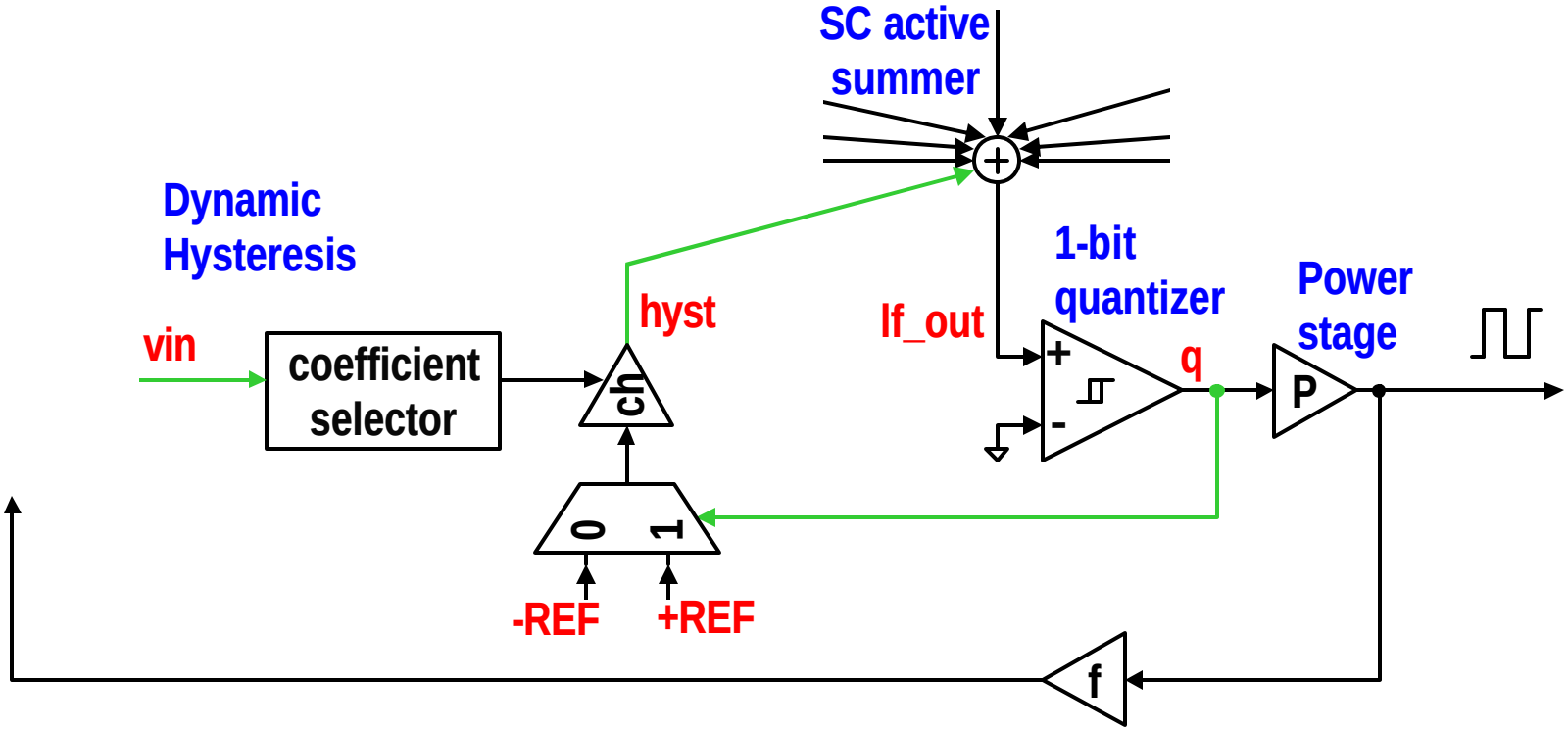
Modulator: (Dynamic quantizer hysteresis)



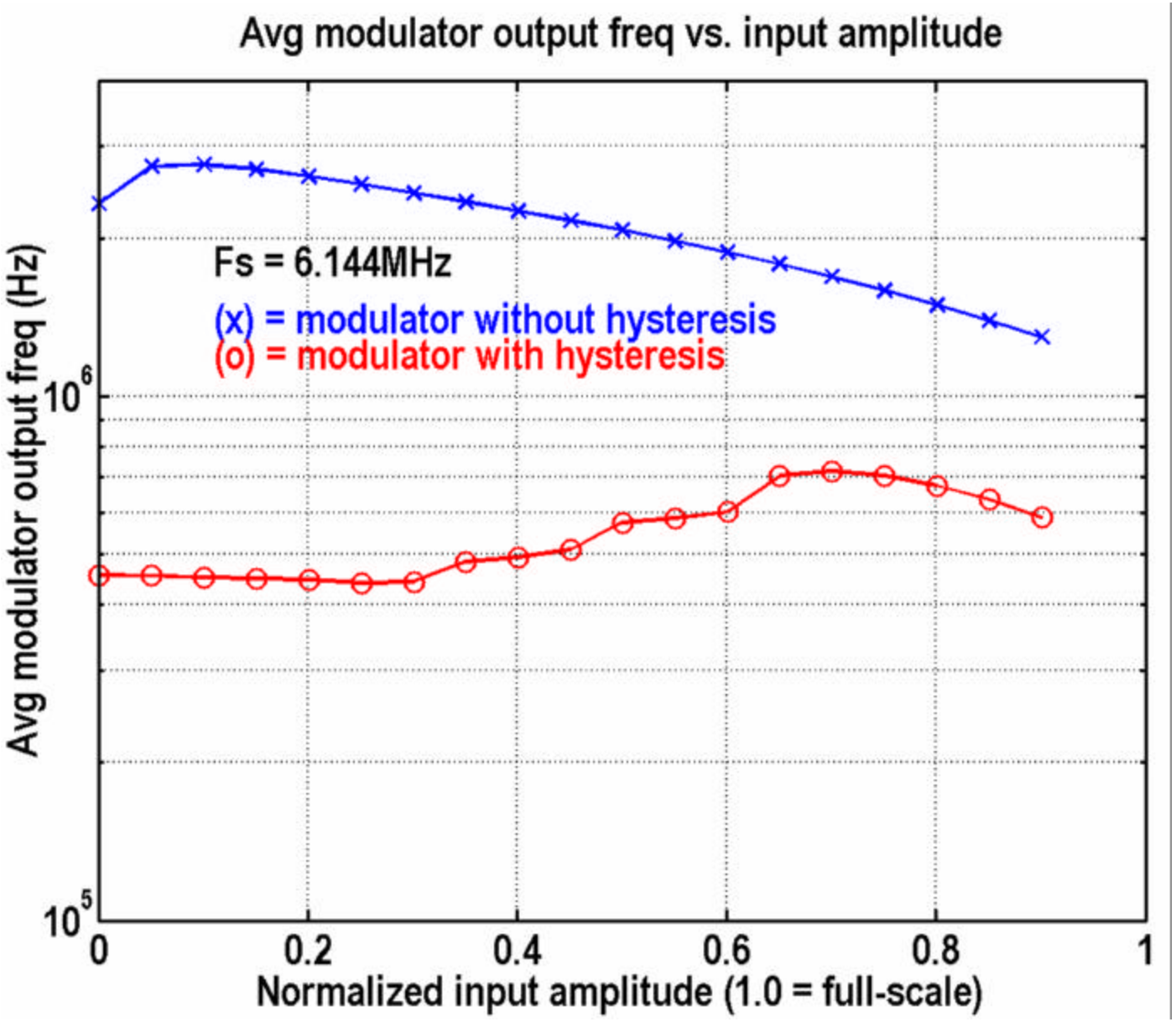
The line shows SNR when a 4-value h(A) lookup table is used.

Modulator: (Dynamic quantizer hysteresis)

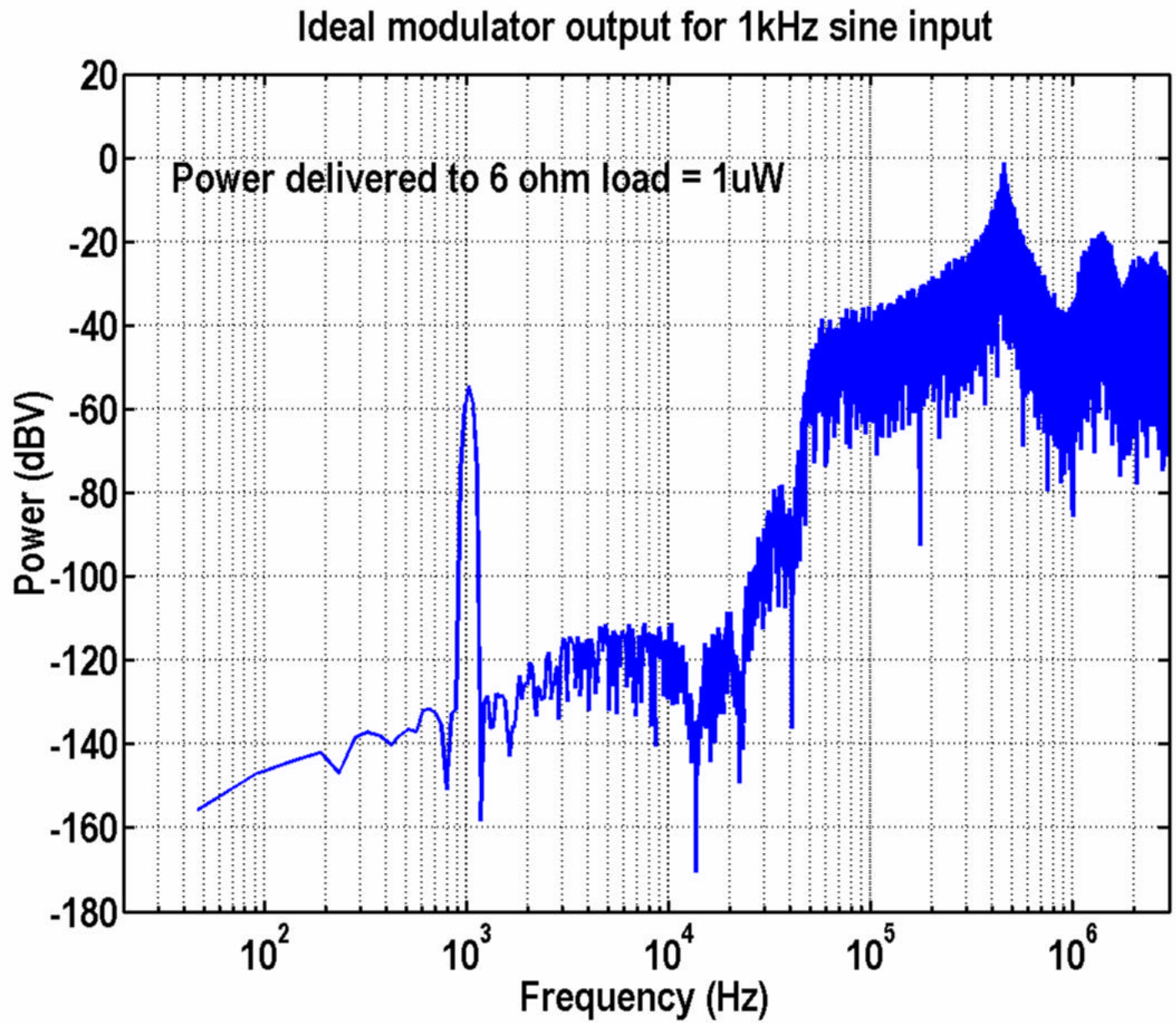
- "Coefficient selector" block implements the h(A) table:
  - bank of 'hysteresis caps' is charged during every SC clock cycle.
  - A 4-level FLASH ADC monitors vin.
  - Logic interprets the FLASH result, determining how many caps to connect to the SC summer, and how many to dump to a throwaway node, giving 4 choices for ch.



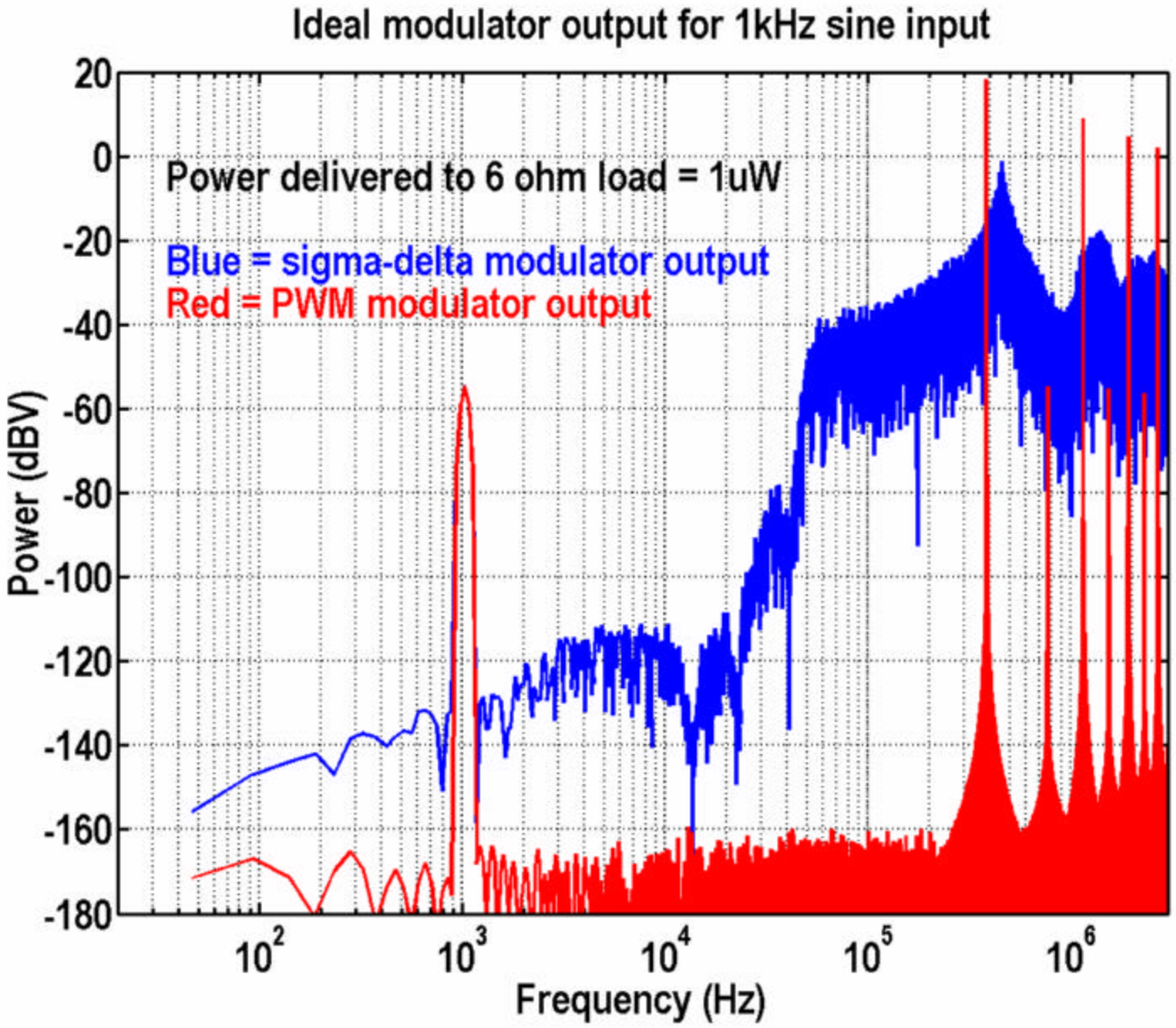
Modulator: (Dynamic quantizer hysteresis)



Modulator: (Output spectrum)

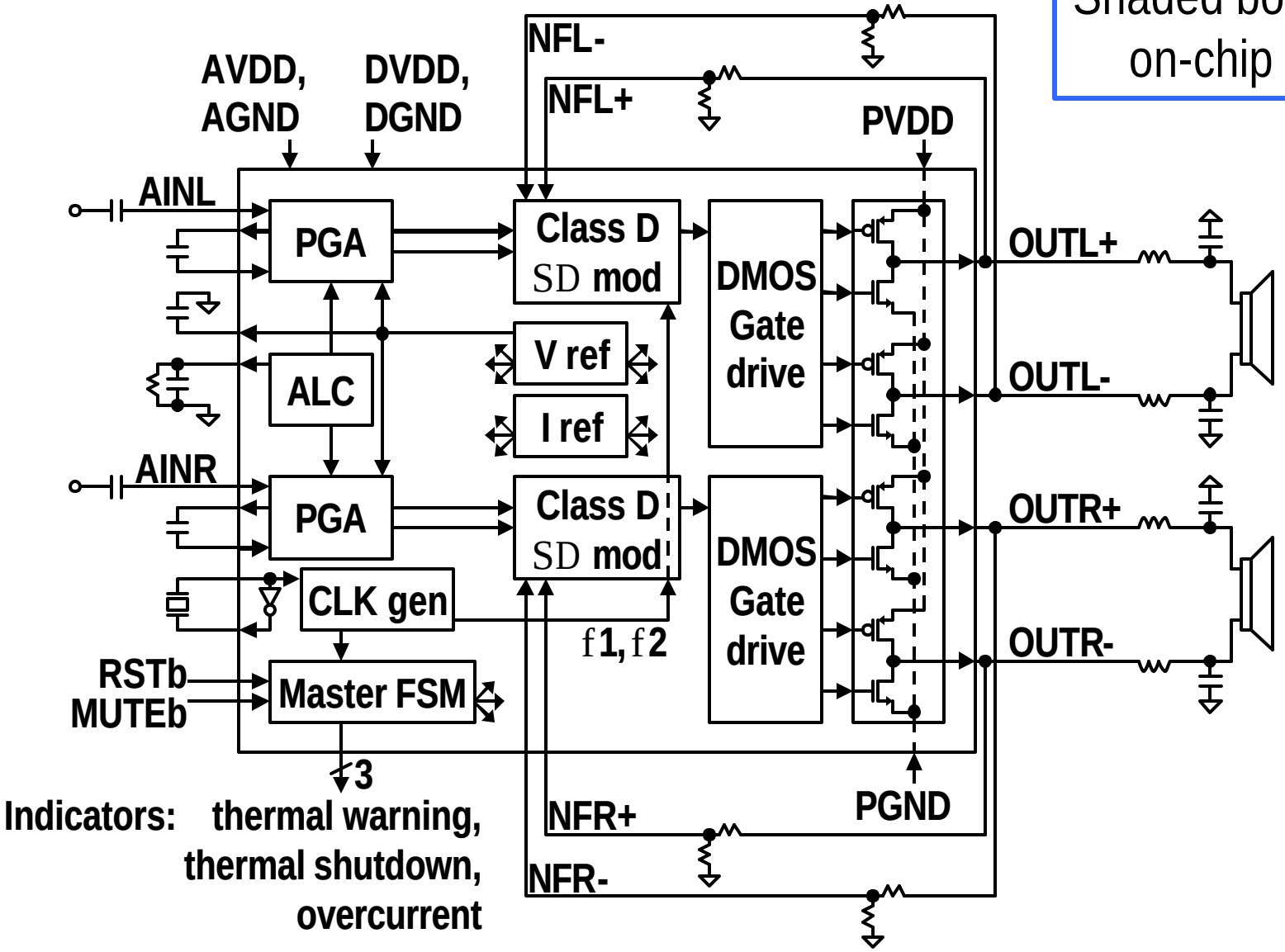


Modulator: (Output spectrum, vs PWM r



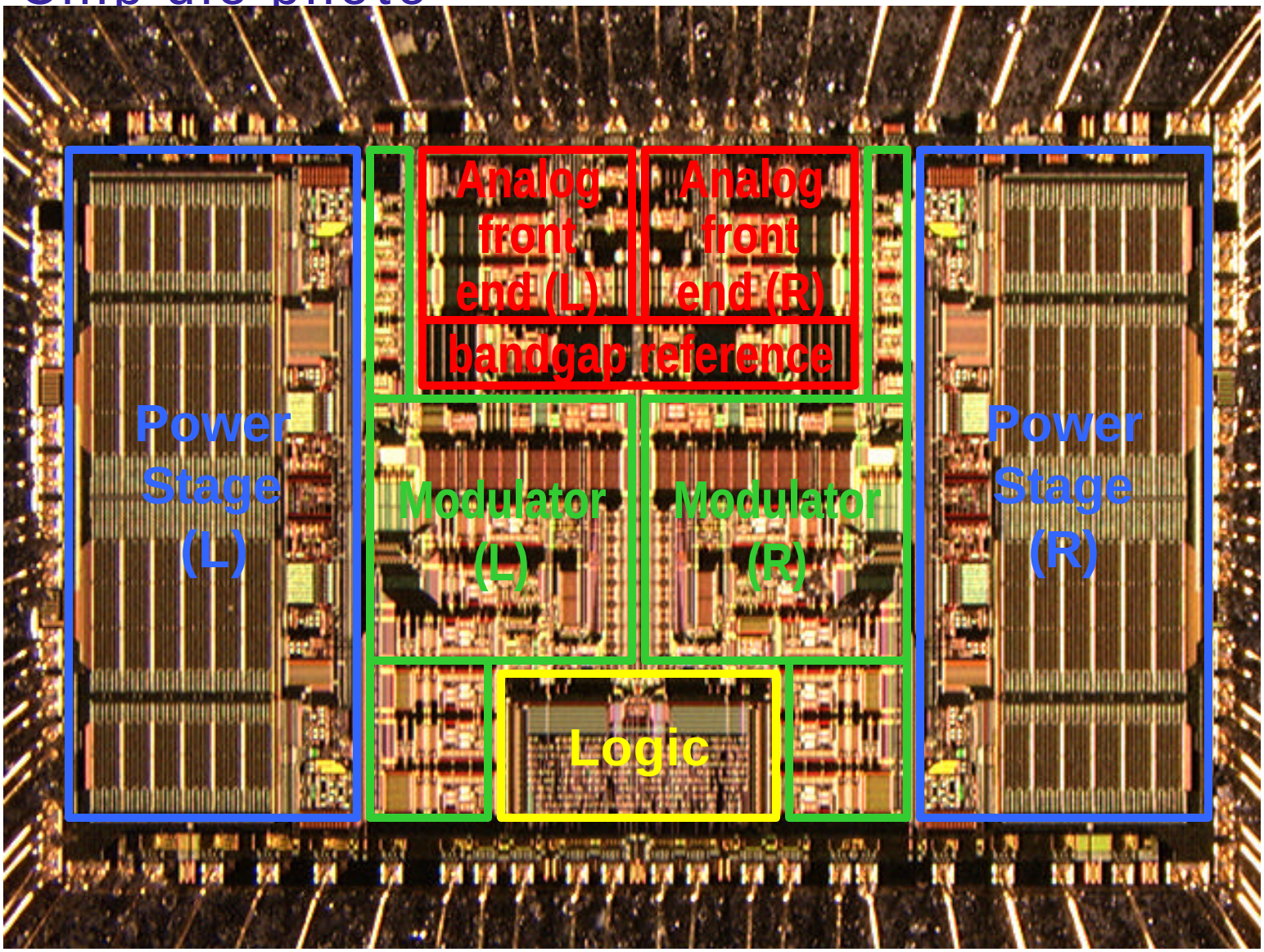
Chip block diagram

Shaded box encloses on-chip circuitry



ANALOG DEVICES

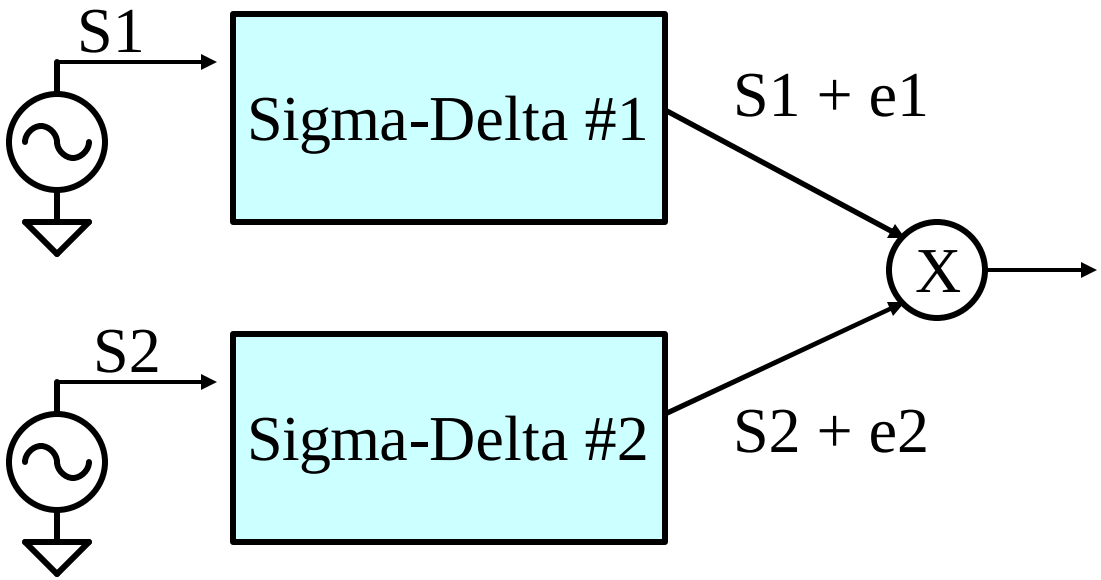
Chip die photo



Outline

- Intro: SAR vs Sigma-Delta
- New conversion architectures driven from practical needs in the integrated circuit industry
  - From 1-bit to Multi-bit
  - Multi-bit Mismatch Shaping
  - Split Noise-shaping – noise-shaped segmentation
  - CT DACs
  - Mixed CT/DT ADCs
- Power Sigma-Delta ("class-D" amplifiers)
  - Using dynamic hysteresis to reduce the output transition rate
- Research work
  - *Multiplying Two 1-bit signals and getting a noise-shaped result*
  - Single-structure sigma-delta/successive-approximation; a converging time-domain view of sigma-delta

Coupled Loops for Multiplication of Two Sigma-Delta Streams



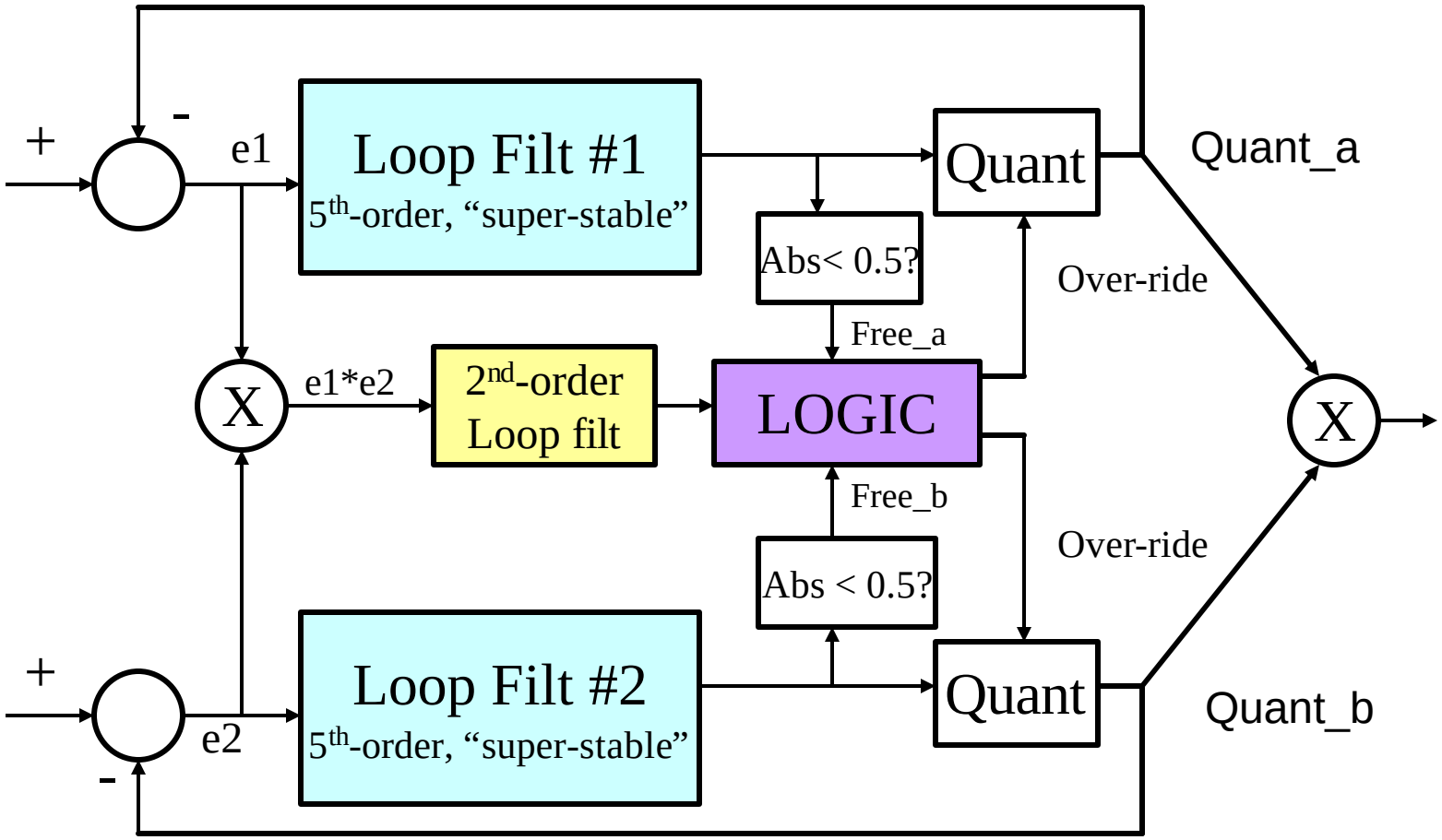
OUT

- S1*S2 + ← Desired signal
- S1*e2 + ← e2 noise-shaping shifted by +/- f1
- S2*e1 + ← e1 noise-shaping shifted by +/- f2
- e1*e2 ← White noise, all noise-shaping components folded down due to multiplication!

Coupled Loops for Multiplication of Two Sigma-Delta Streams

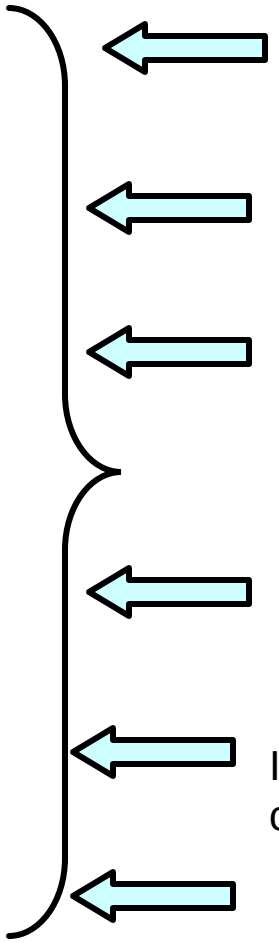
- Highly-stable modulators can tolerate making non-ideal quantization decisions fairly often.
- We can use this fact to cause the high-frequency shaped noise between two separate modulators to become correlated.
- This correlation can result in the product of two 1-bit streams to also be noise-shaped.

Implementation



Logic Implementation

```
if((quant_a == quant_b) && (loop_filt_2ndord > 0.0)) {
                    if(free_a == 1) {
                                quant_a = -quant_a;
                    } else if(free_b == 1) {
                                quant_b = -quanta_b;
                    }
          }
if((quant_a == -quanta_b) && (loop_filt_2ndord < 0.0)) {
                    if(free_a == 1) {
                                quant_a = -quant_a;
                    } else if(free_b == 1) {
                                quant_b = -quant_b;
                    }
          }
```



Next decision will be quant_a = quant_b, but 2nd-order loop would like quant_a != quant_b

If quant_a is “free”, change it

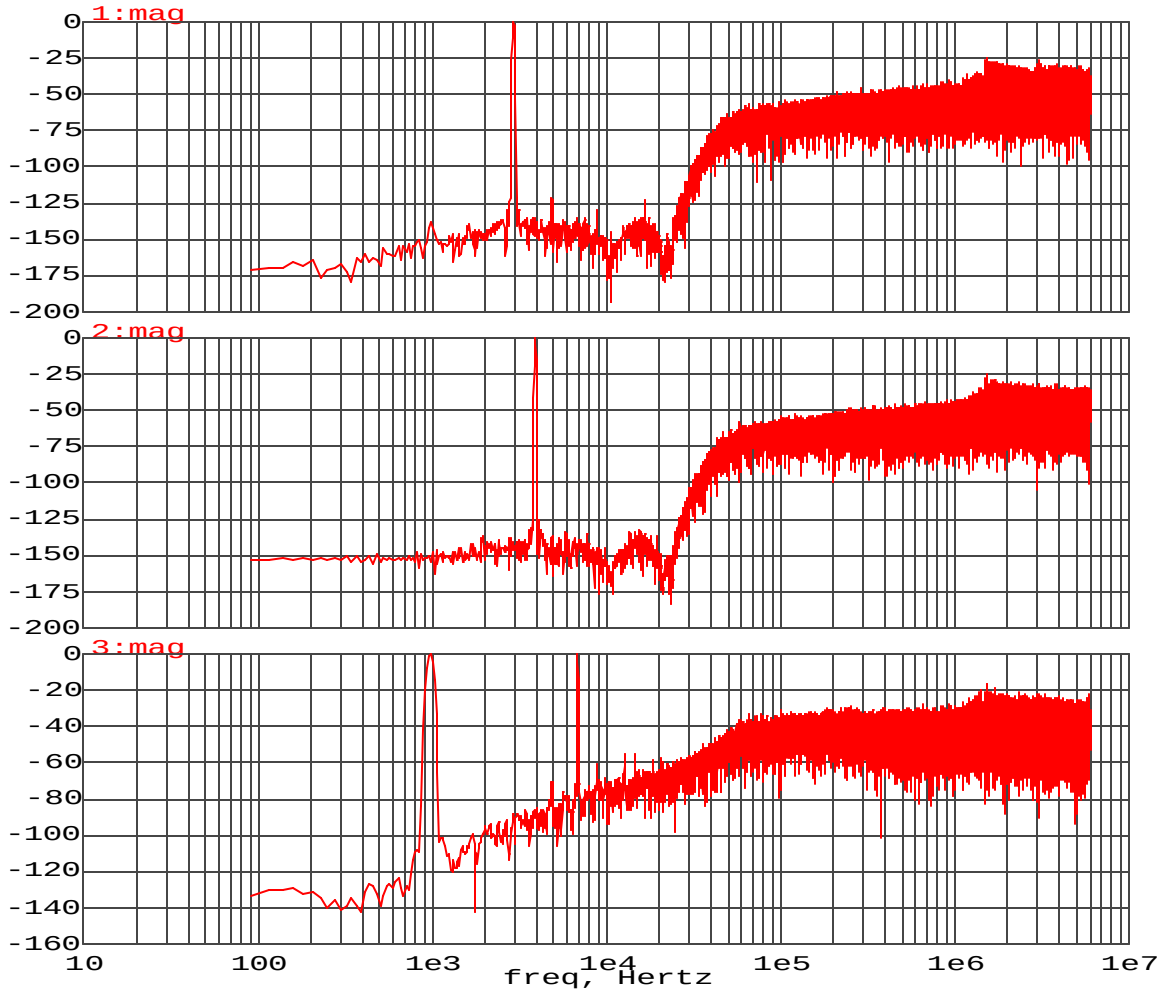
If quant_b is “free”, change it

Next decision will be quant_a != quant_b, but 2nd-order loop would like quant_a = quant_b

If quant_a is “free”, change it

If quant_b is “free”, change it

Simulation Results, C-code



FFT of sigma-delta #1, 3 KHz input

FFT of sigma-delta #2, 4 KHz input

FFT of product.

Sum and difference frequencies clearly visible

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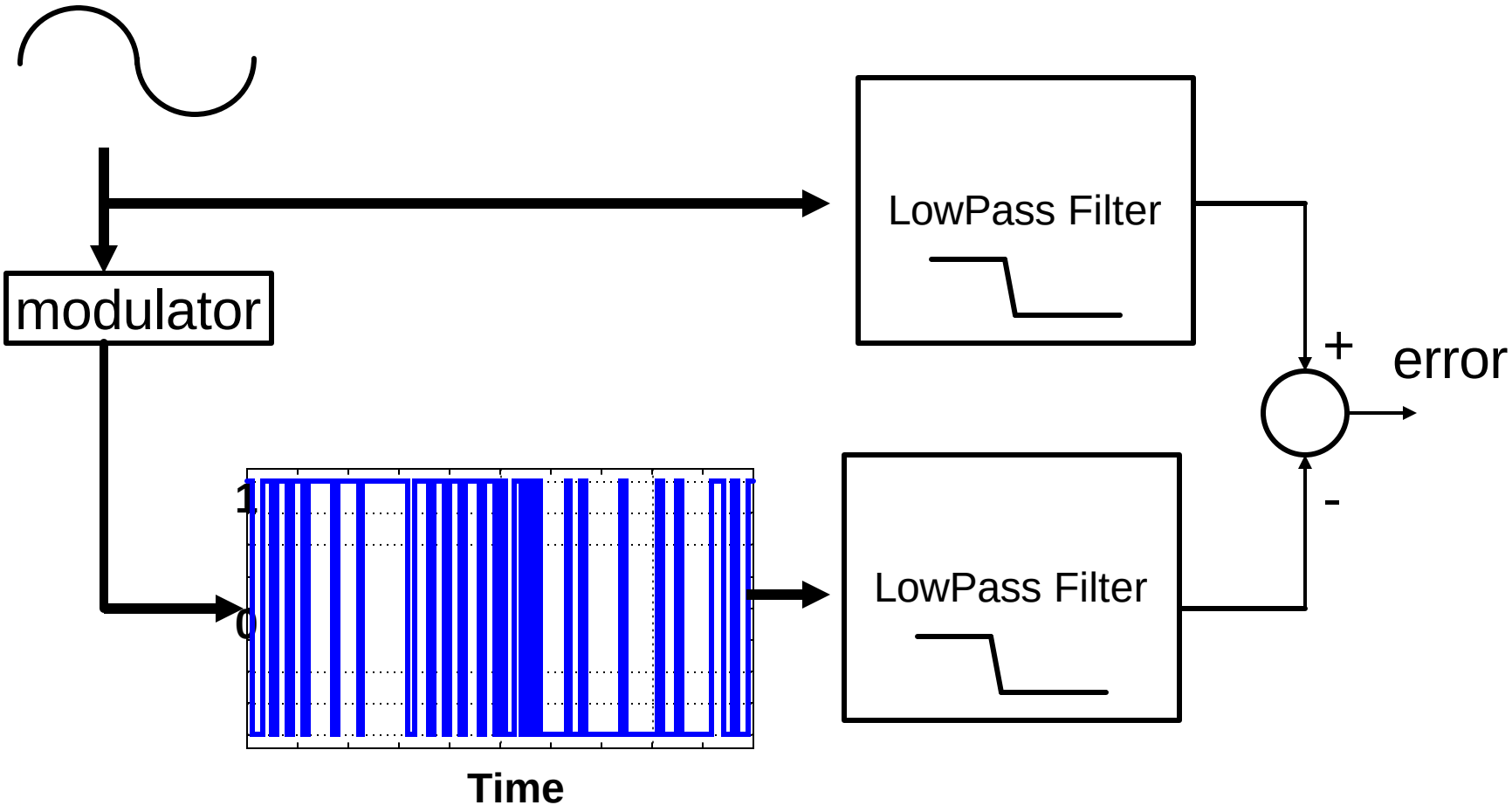
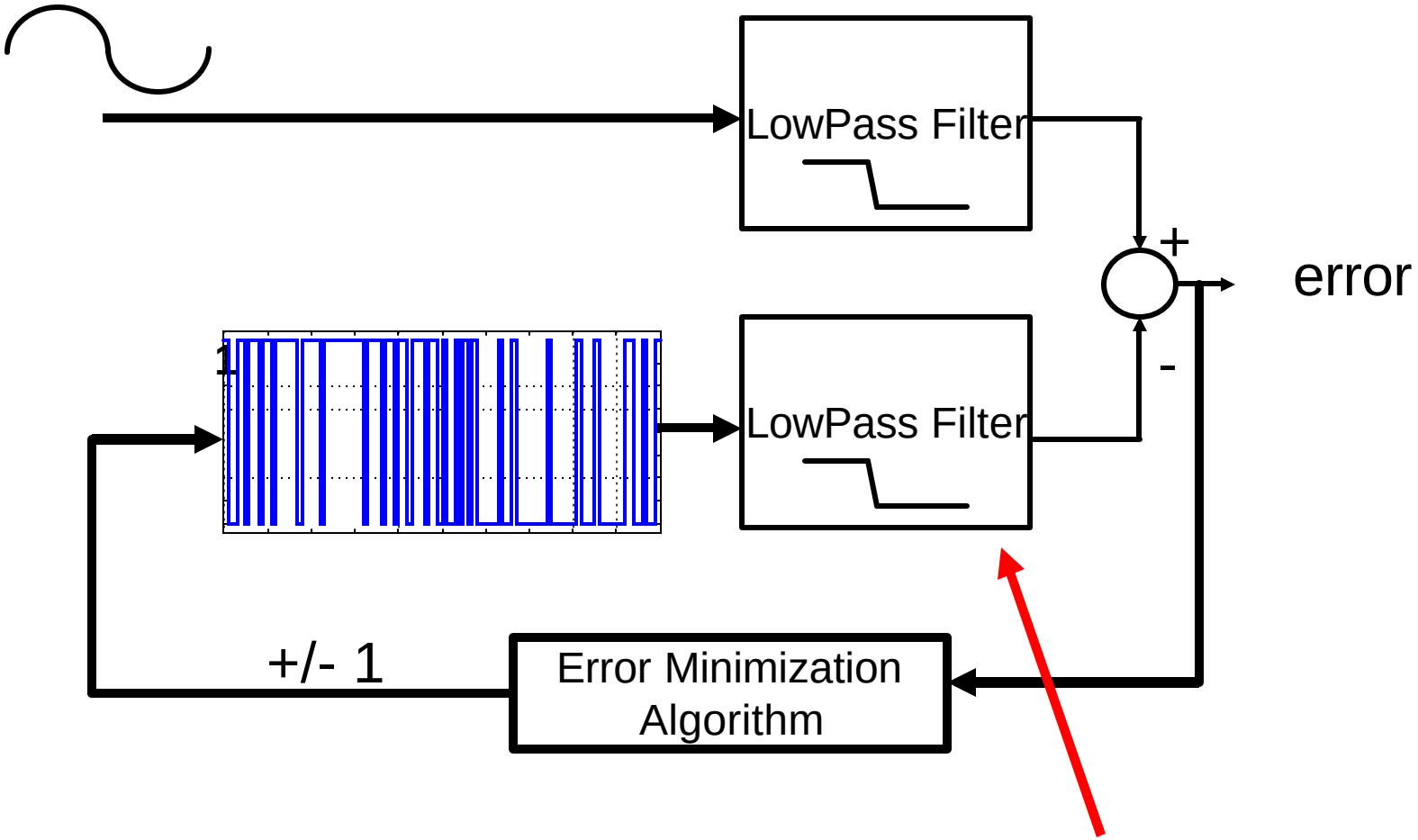
Can we view ΔΣ as a "Converging Algorithm"?

- Traditionally, "successive-approximation" converters are viewed as a converging series of approximations in the time domain, whereas ΔΣ converters are viewed in the frequency domain.
- However, after brick-wall filtering, the time-domain error between the filtered bit-stream and an identically-filtered input becomes very small.
- Can we take a similar time-domain view of ΔΣ ?
- Yes, but it must be viewed a "successive-waveform-approximation" ; the optimization is done on large groups of samples rather than individual samples!

Time-domain Error Concept

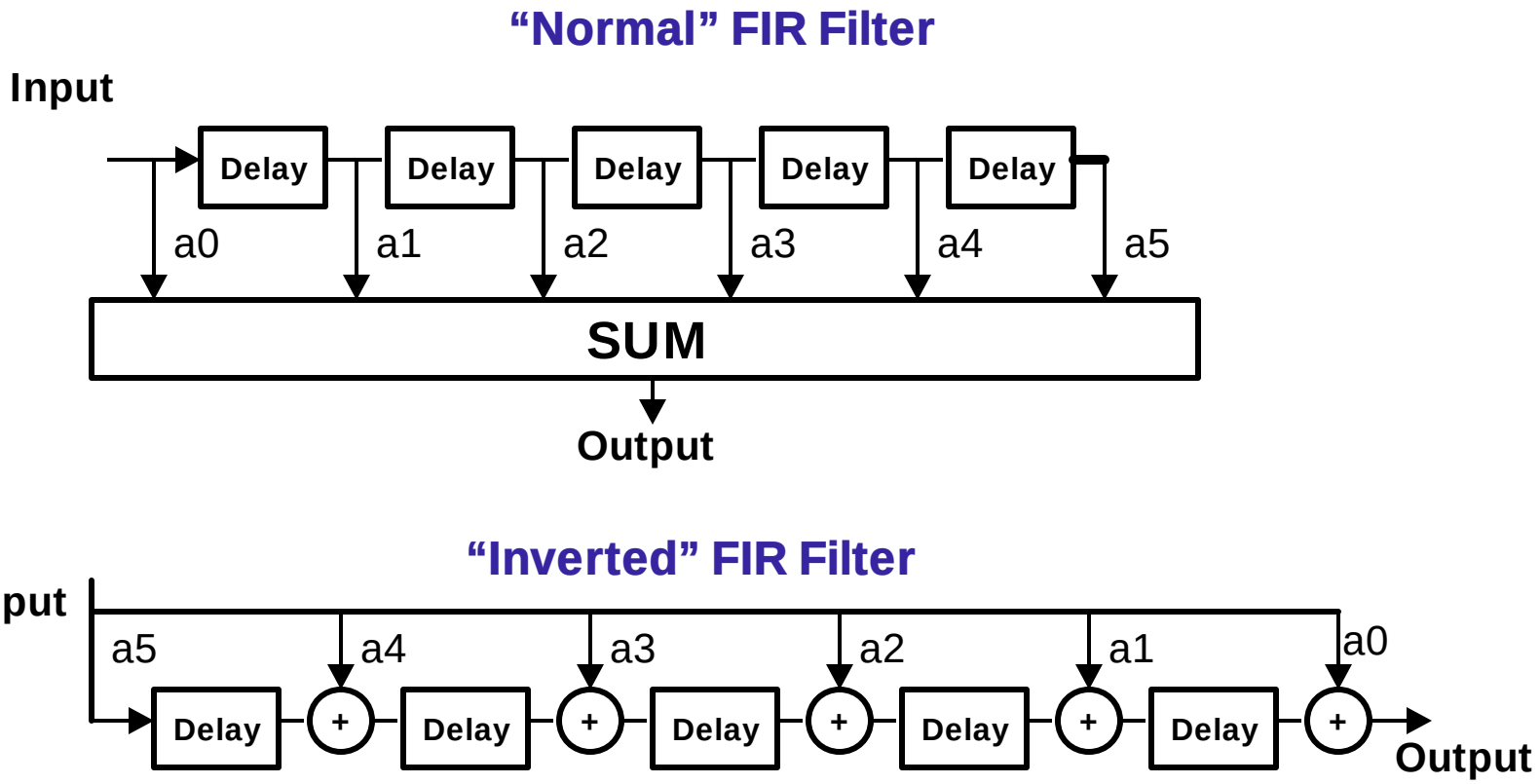


Closing the Loop around the Brickwall filter; the Impossible Dream!



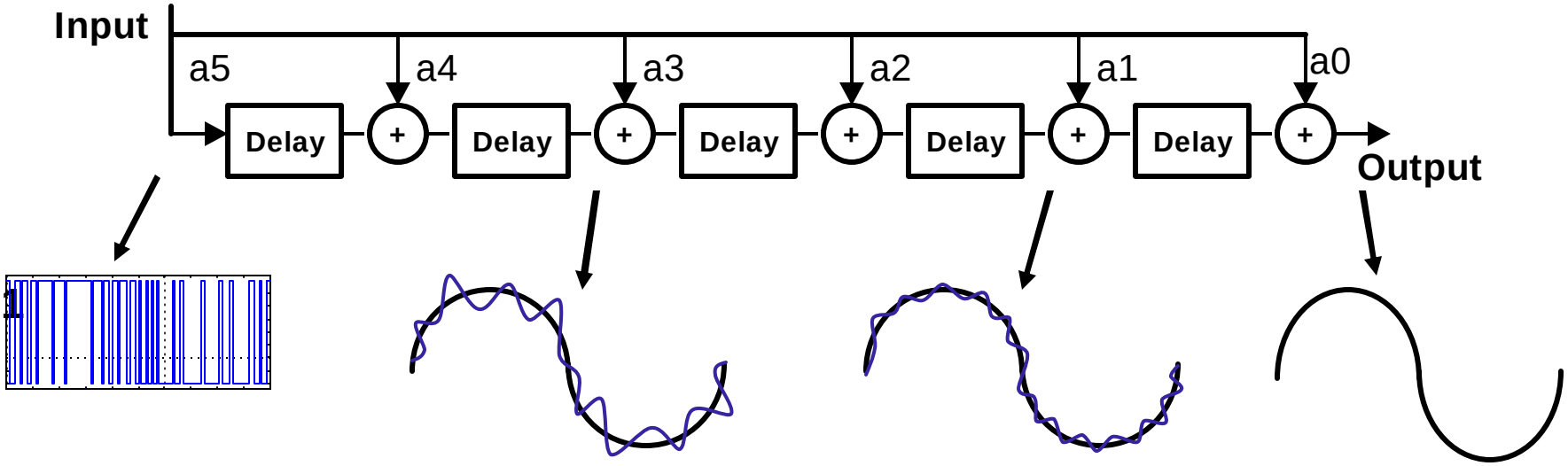
This filter has FAR too much delay; closing the loop will cause instability!

Can One Structure do both SAR and ΔΣ?



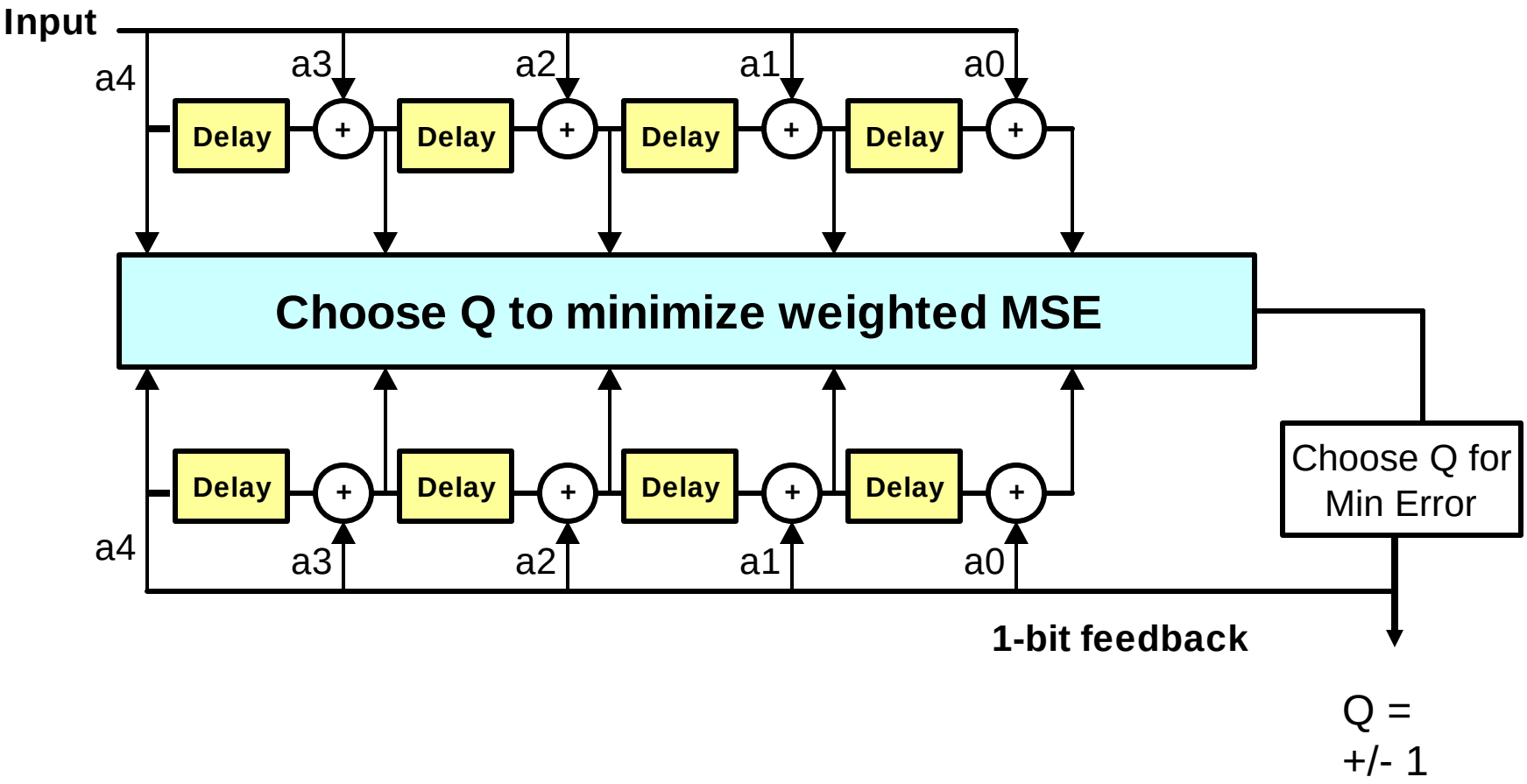
The "inverted" form shows the progression of changes that an input experiences on its way through the shift register. The normal form does not.

Can One Structure do both SAR and ΔΣ?

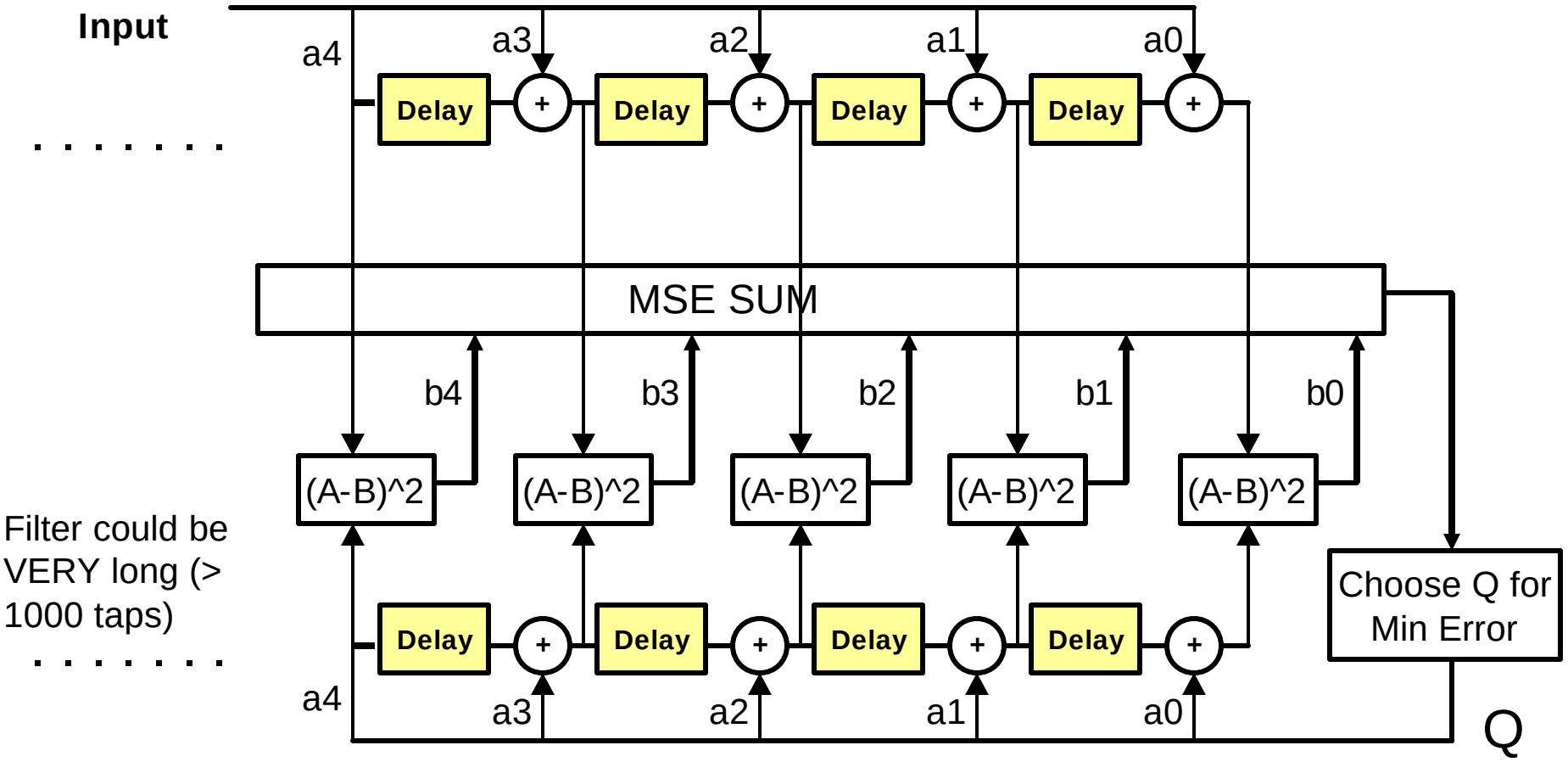


Progressive filtering of the inverted FIR form

Can One Structure do both SAR and ΔΣ?

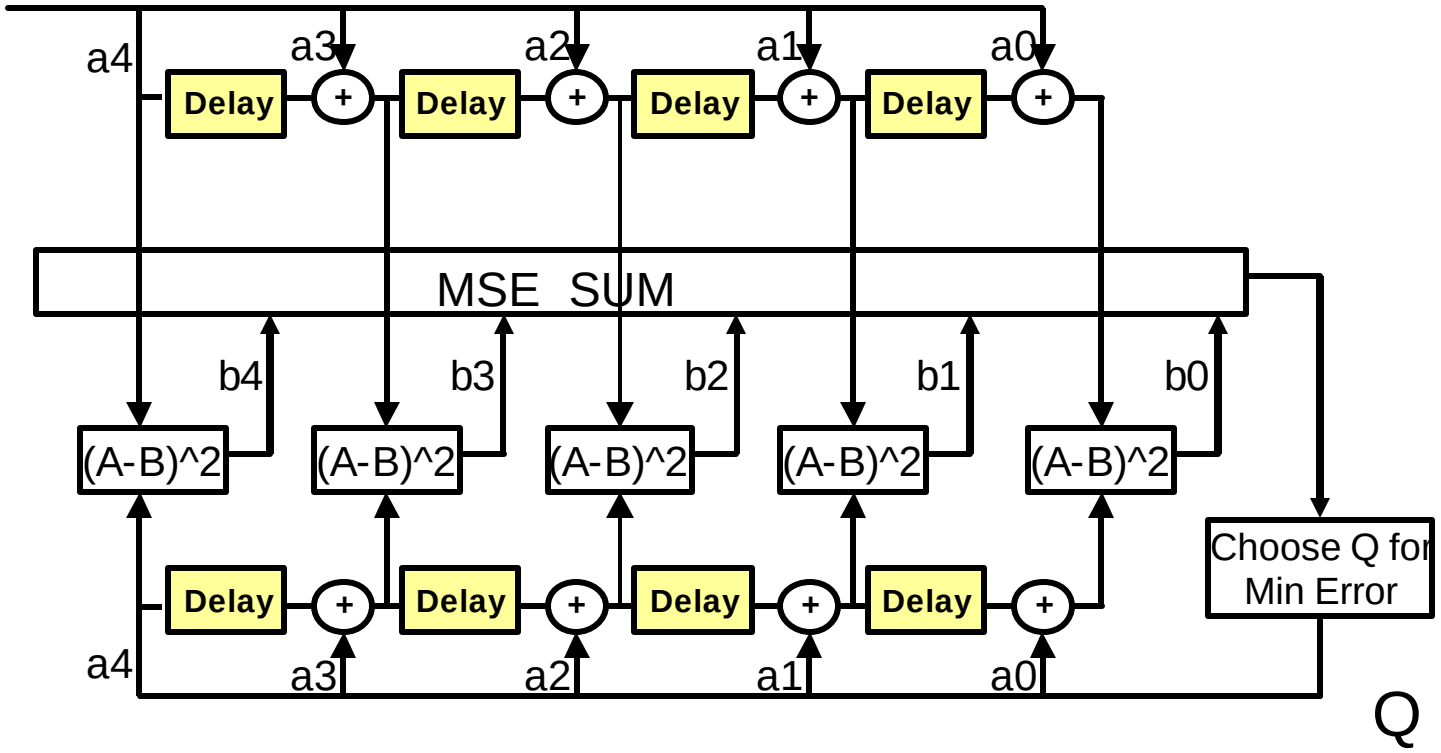


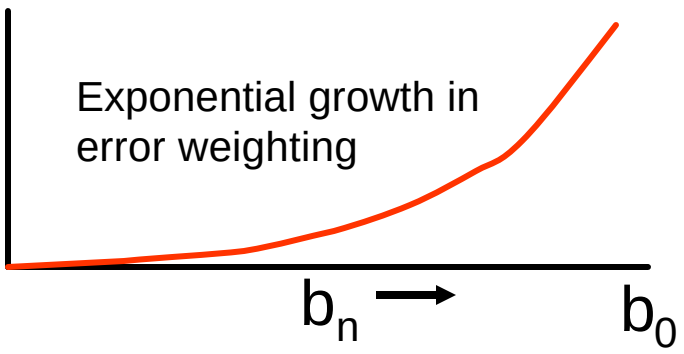
ΔΣ View

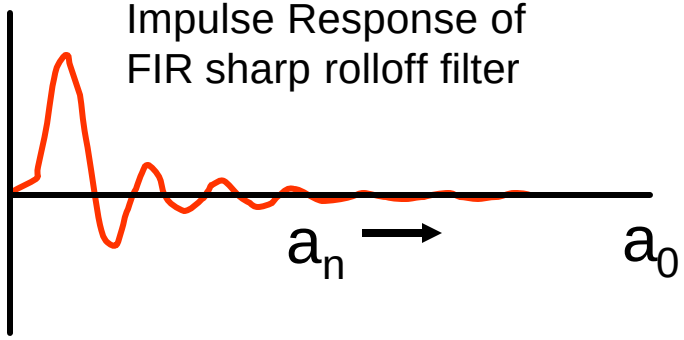


Filter could be VERY long (> 1000 taps)

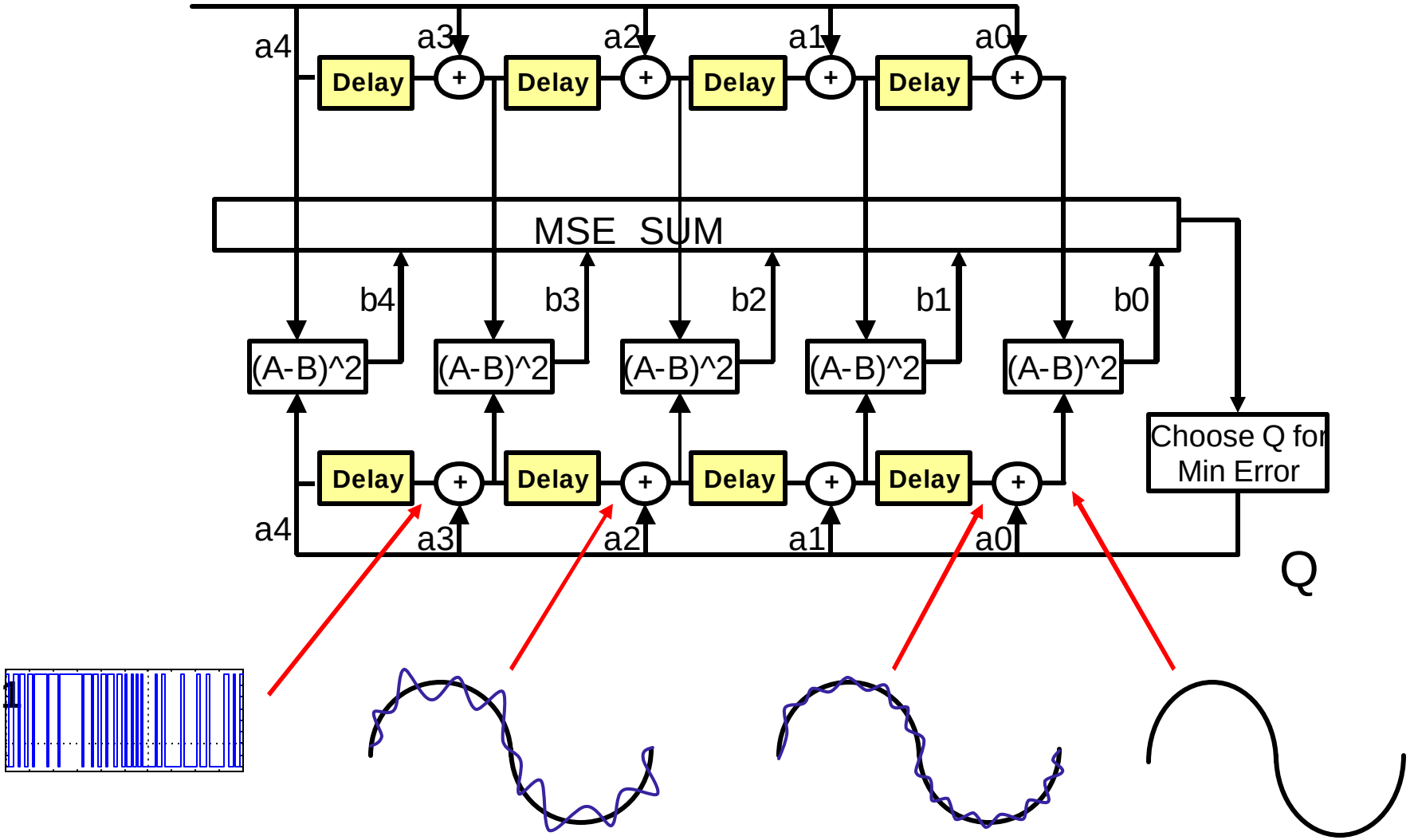
ΔΣ View



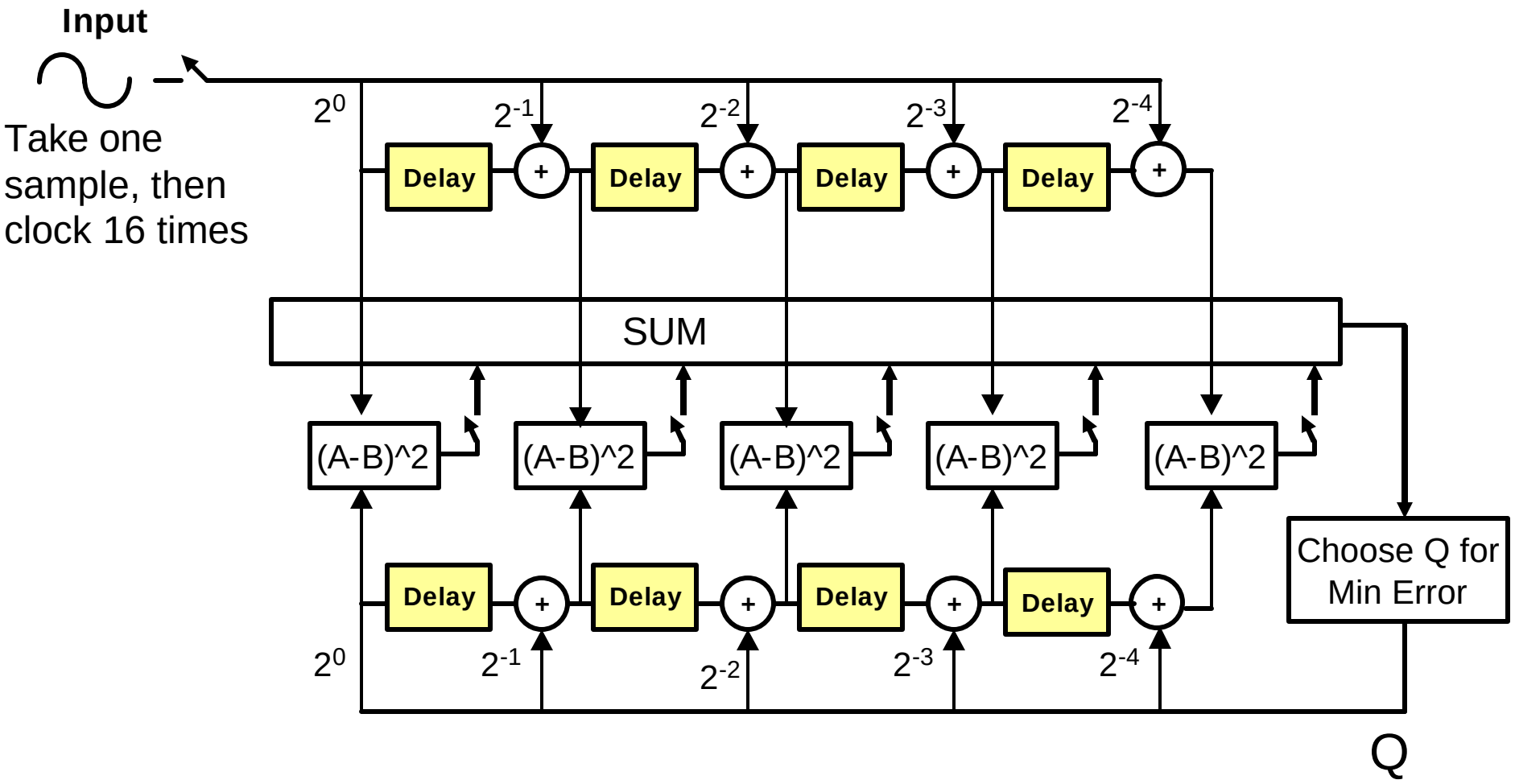




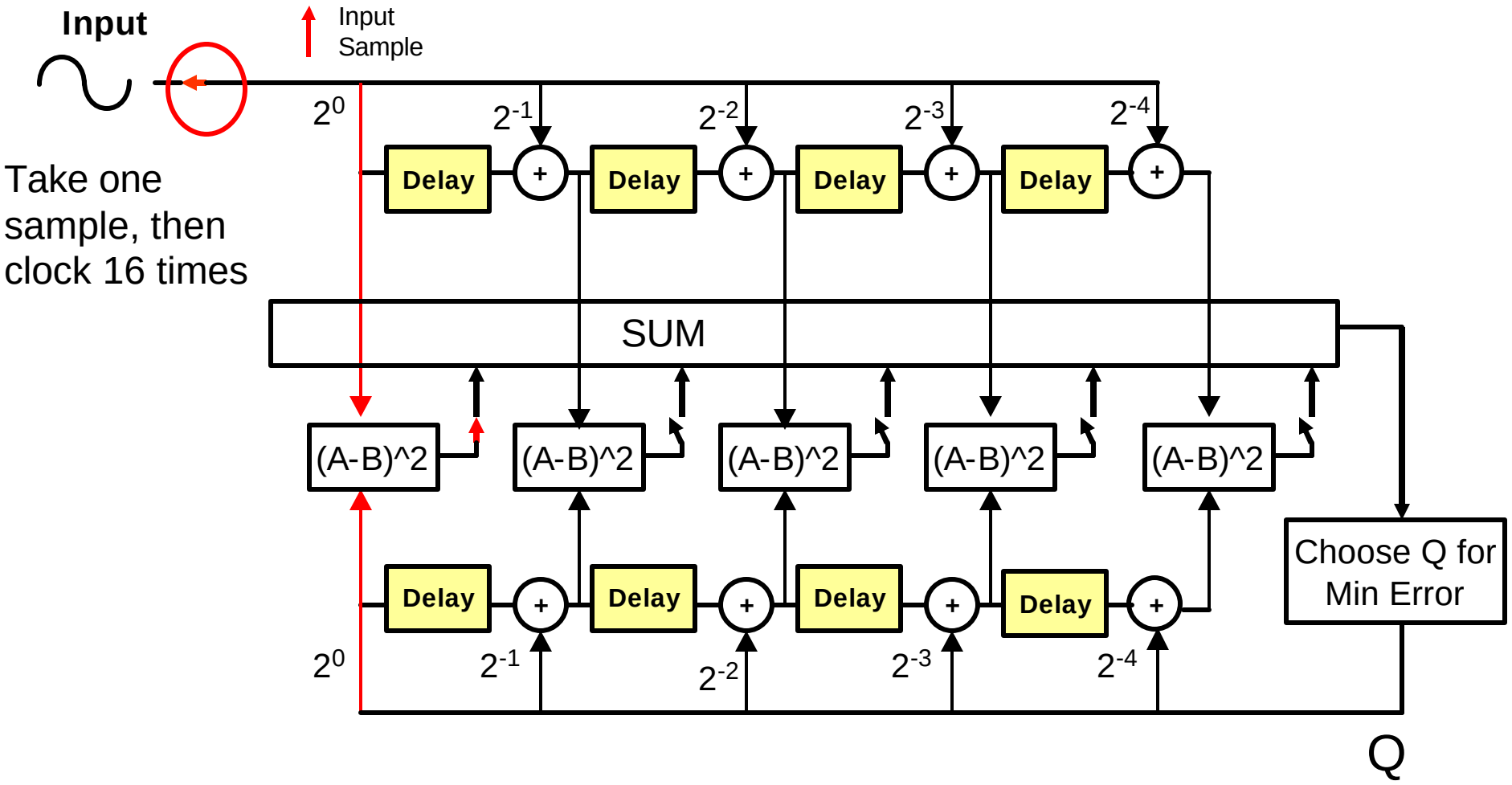
ΔΣ View



Operation as a Successive-approximation Converter



Operation as a Successive-approximation Converter



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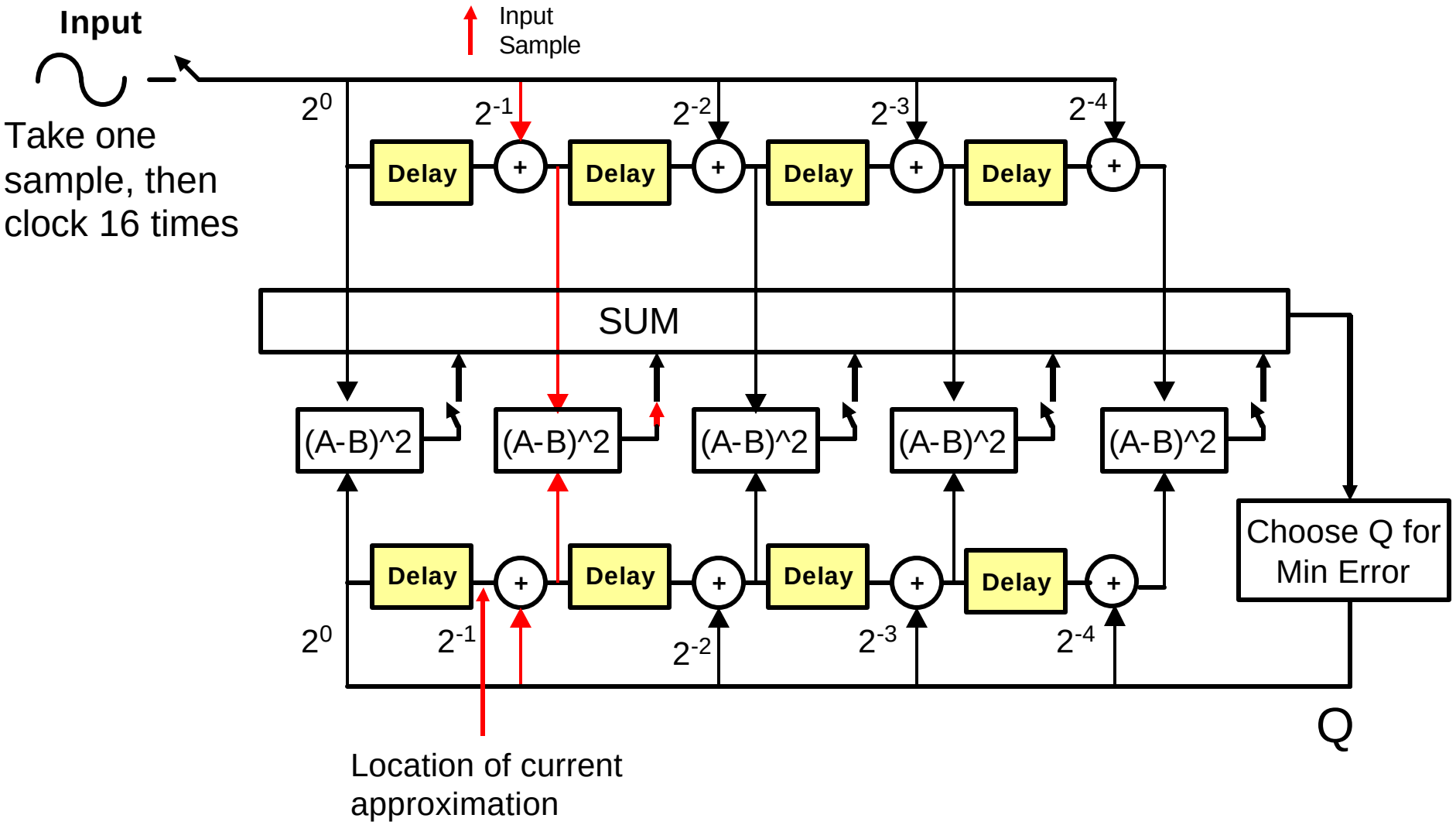

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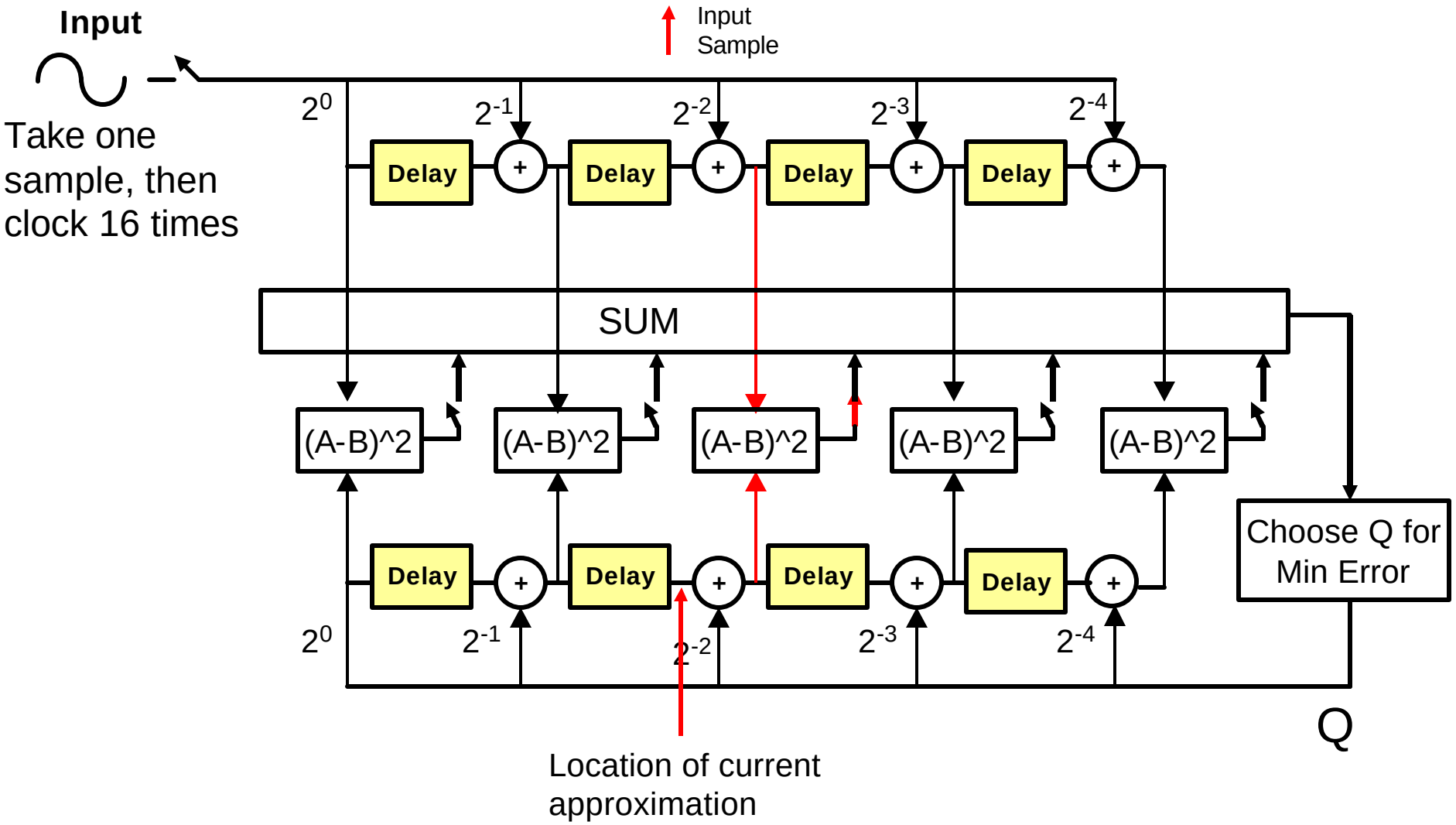

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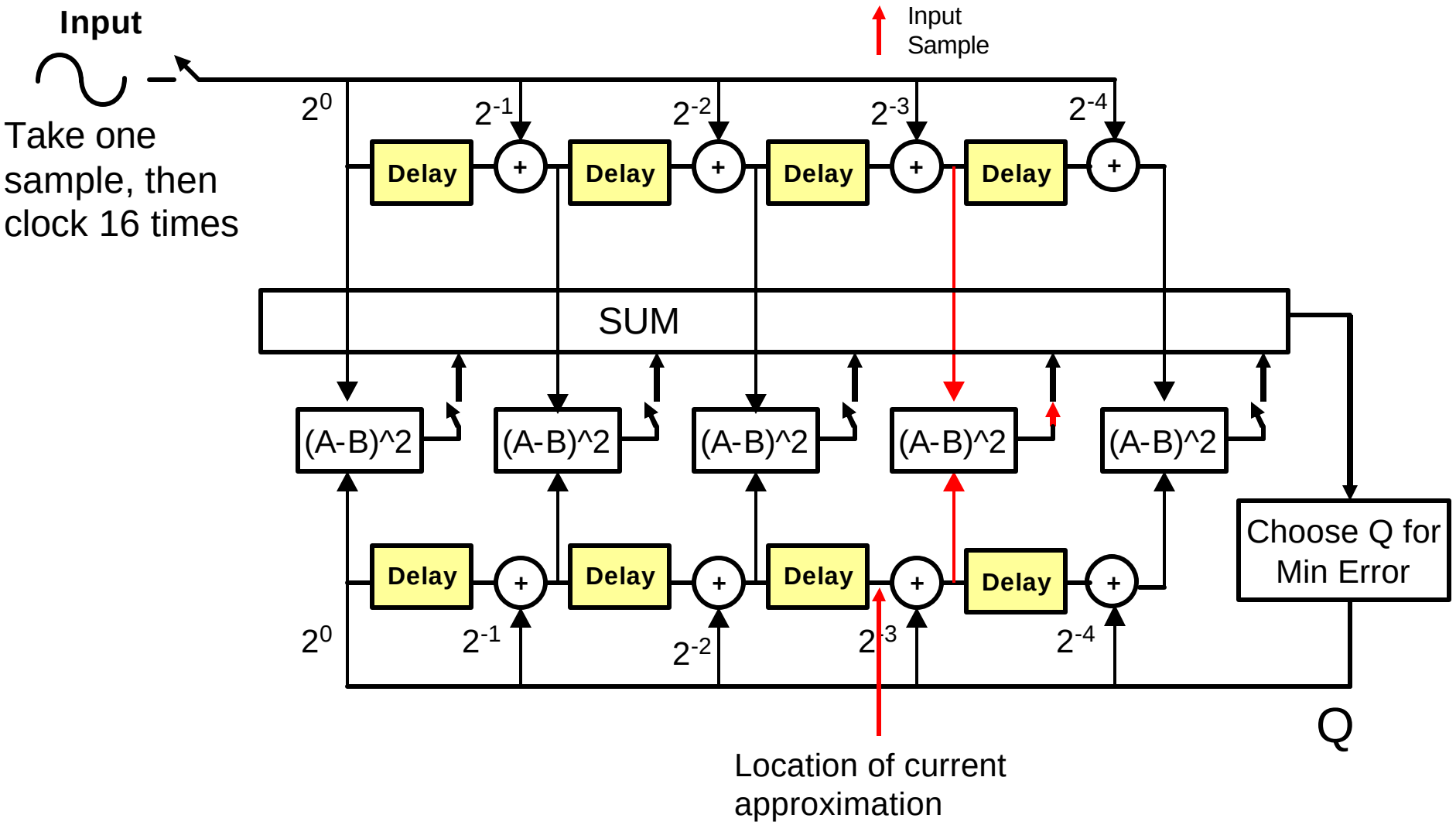

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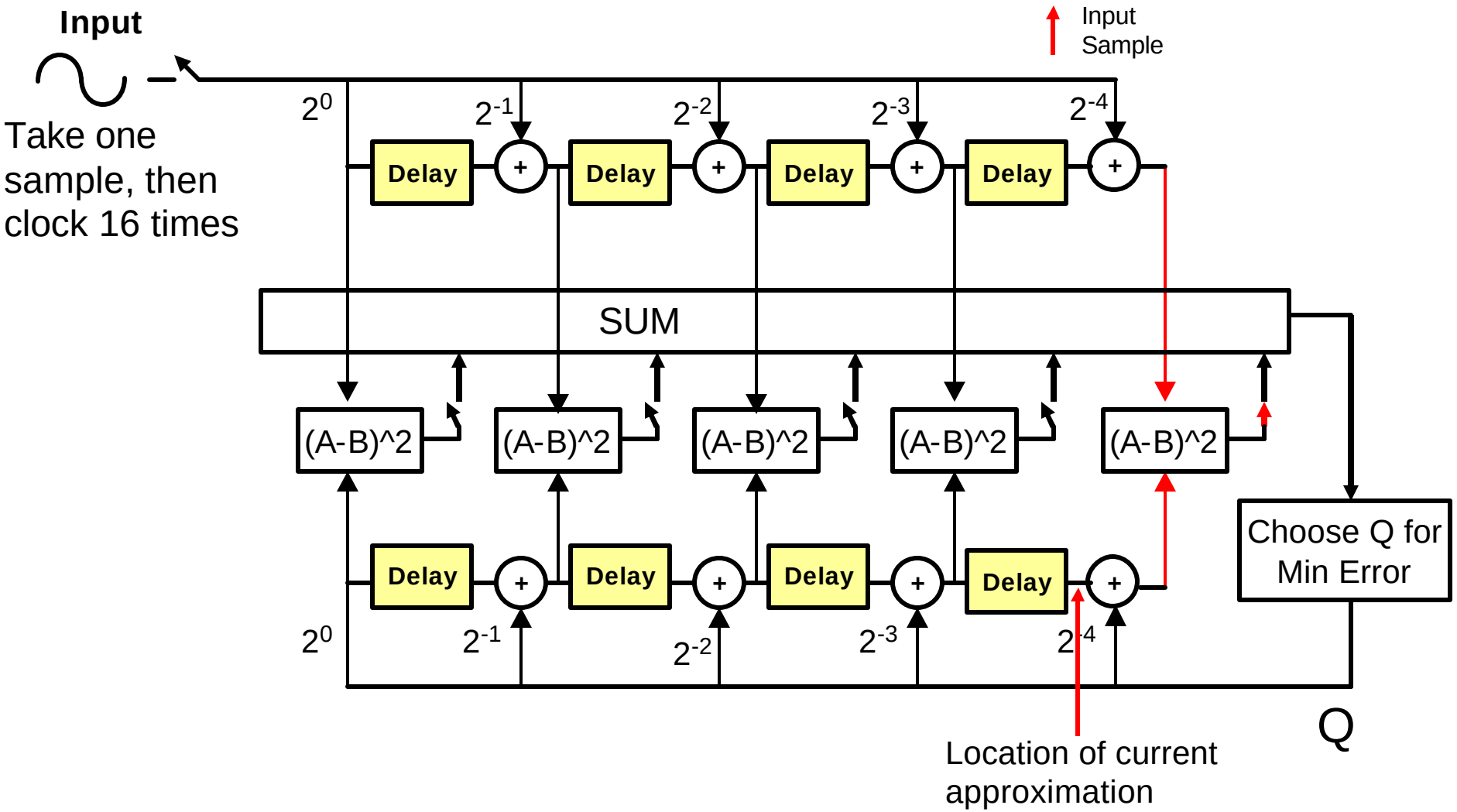
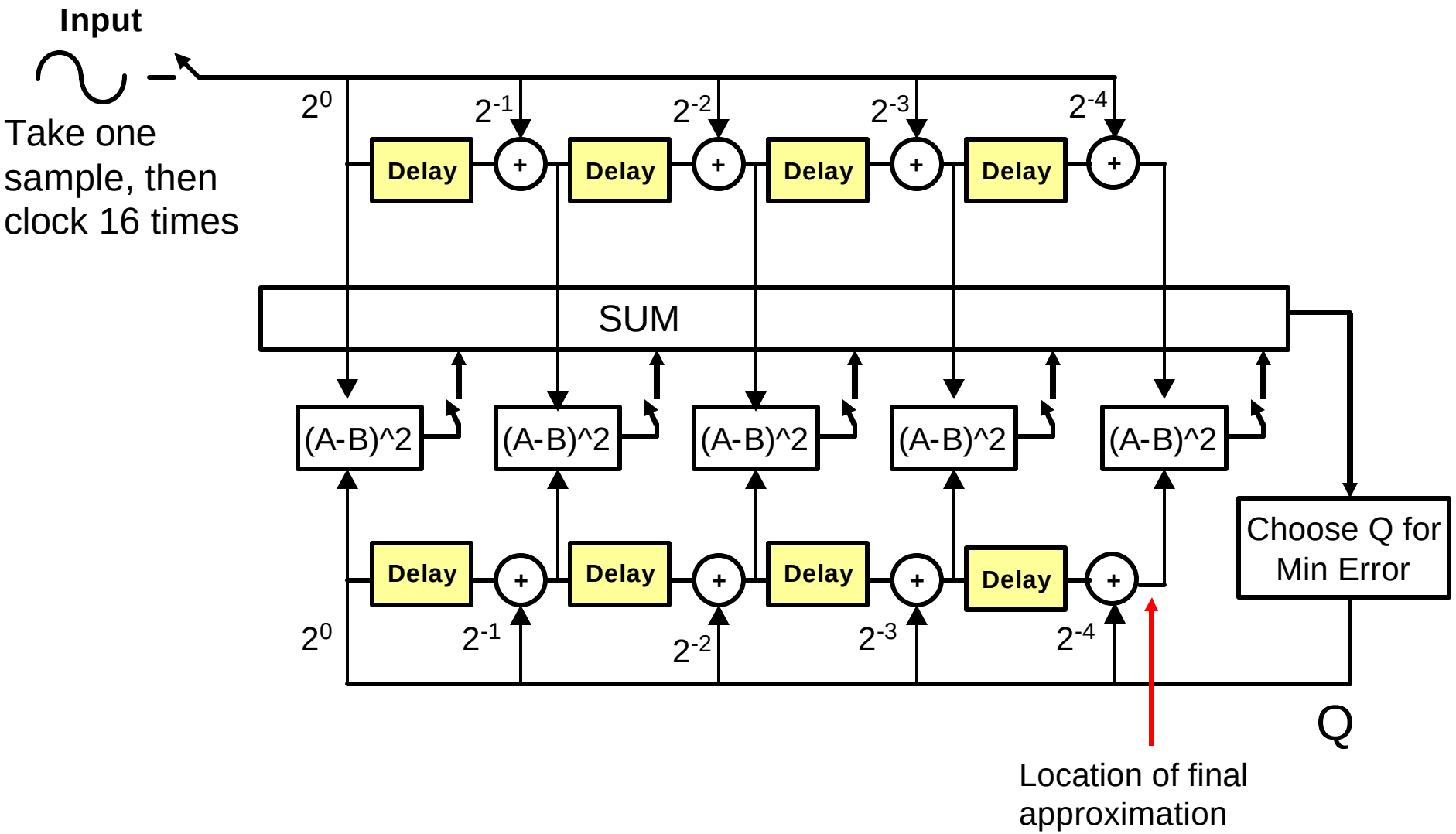


ANALOG DEVICES

Operation as a Successive-approximation Converter



Can One Structure do both SAR and ΔΣ?

SAR VIEW:

- **The shift-register feed-in weights are weighted with 2^N weightings.**
- **A single sample is taken and entered into the shift register. All other input samples are 0.**
- **As this sample is shifted through, the Magic Box compares the estimated value shifting through the lower shift-register to the value shifting through the upper shift register. It makes a 1-bit decision based on the difference.**
- **The error decreases by about 2X/stage as the estimated value travels from left to right.**

Can One Structure do both SAR and ΔΣ?

Sigma-delta VIEW:

•The shift-register feed-in weights are weighted with lowpass filter coefficients.

•The oversampled input samples are entered into the top shift register.

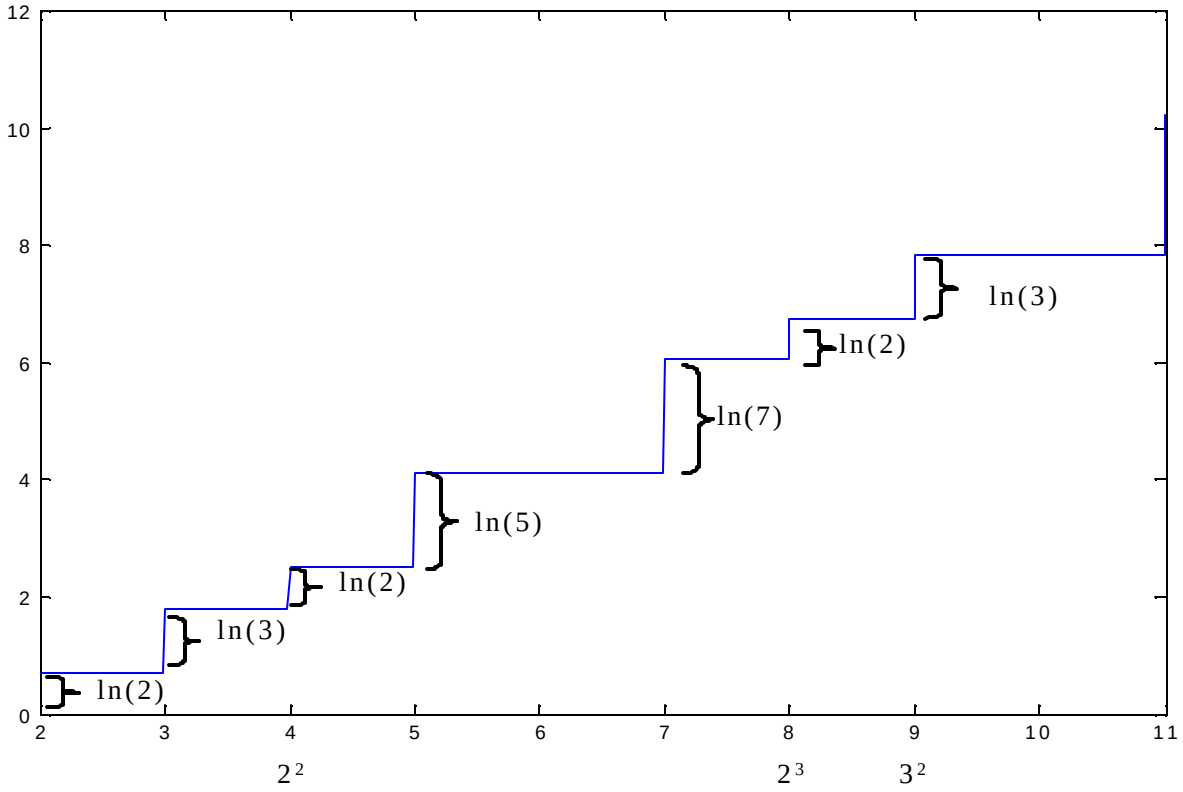
•As these samples shift through the register, the Magic Box looks at difference between ALL of the pairs of shift-register taps to make its 1-bit decision. The errors are large in the early taps and become increasingly small as you move to the right. Stability arises from the fact that you have ADVANCE WARNING that the system will become unstable due to the buildup of errors as you move from left to right in the shift-register.

•Advantage of this technique; the optimization attempts to minimize the difference between the filtered input and the filtered 1-bit stream in a single step. "Normal" sigma-delta does this in 2 steps; the "modulator" is followed by the "decimator". Also, stability is improved with the right "magic box" algorithm.

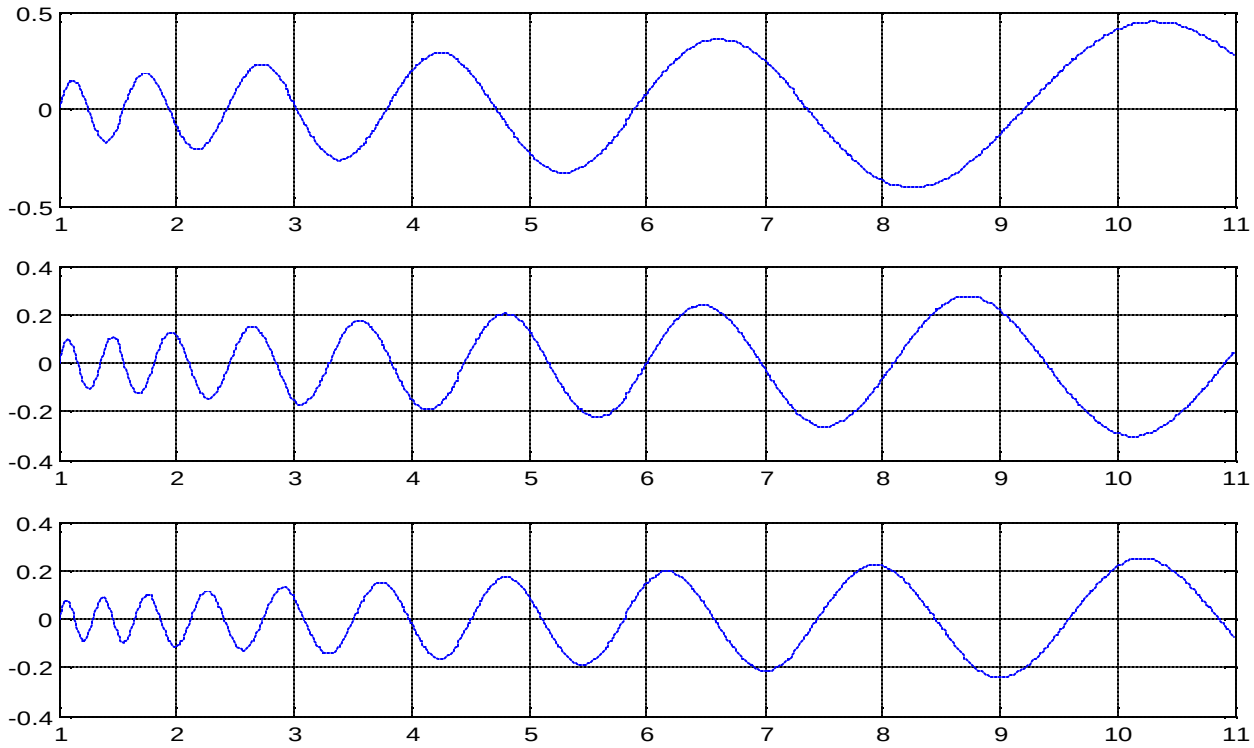
Addendum; you find noise-shaping in the strangest places!

- The prime counting function can be written as a sum of sinusoids with frequencies given by the zeros of the Zeta function.
- The sinusoids, when “sliced vertically”, yield other sinusoids buried in shaped noise!

Chebychev Prime Counting Function $y\,(x)$

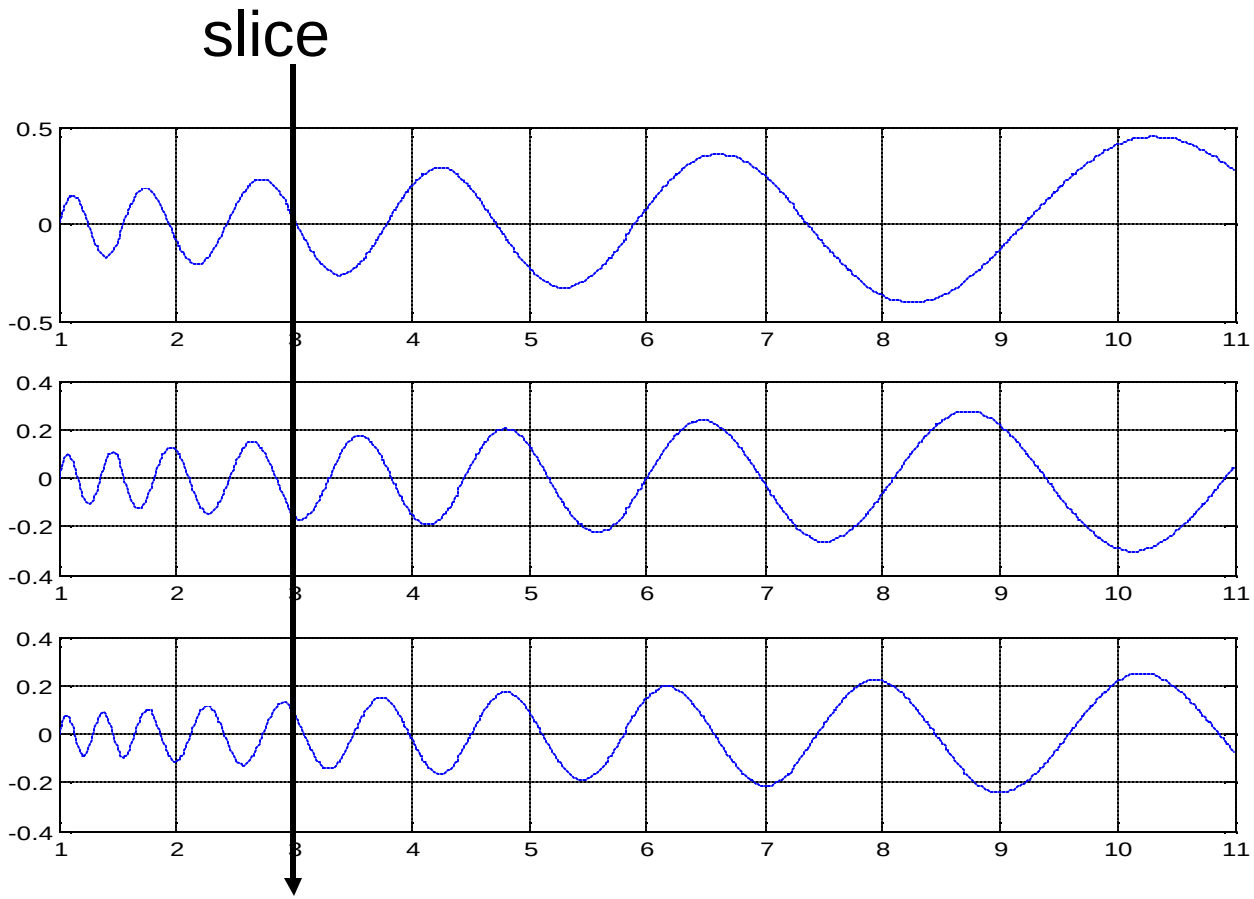


Question; if these waves add up to make steps at primes (and powers of primes) then why do they visually seem to be random at the prime points?



First three terms of the summation $\sum_r \frac{x^r}{r}$

Let’s take a “slice” at 3 and look in the frequency domain



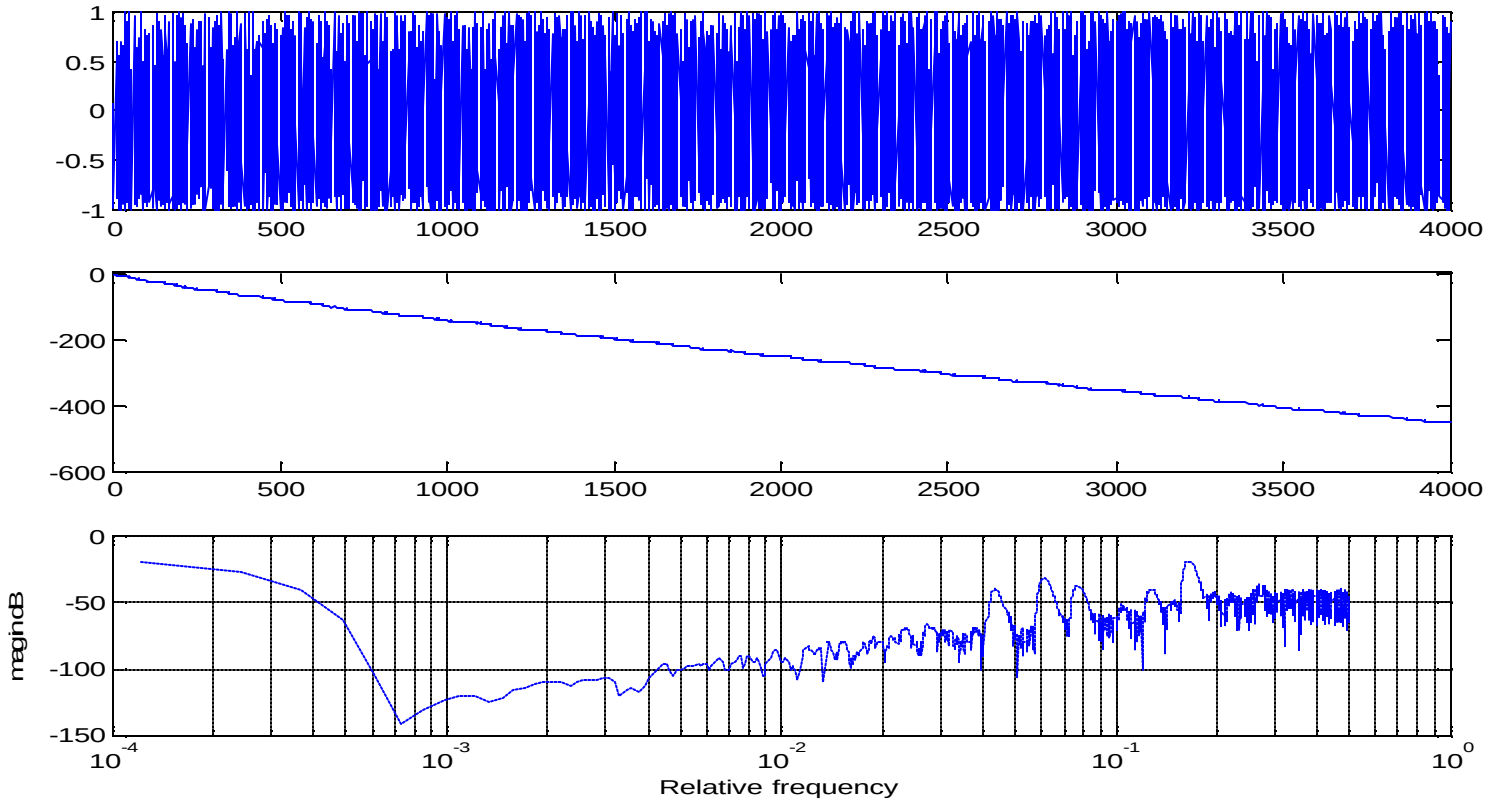
First three terms of the summation $\sum_r \frac{x^r}{r}$

Slice at 3

a)

b)

c)

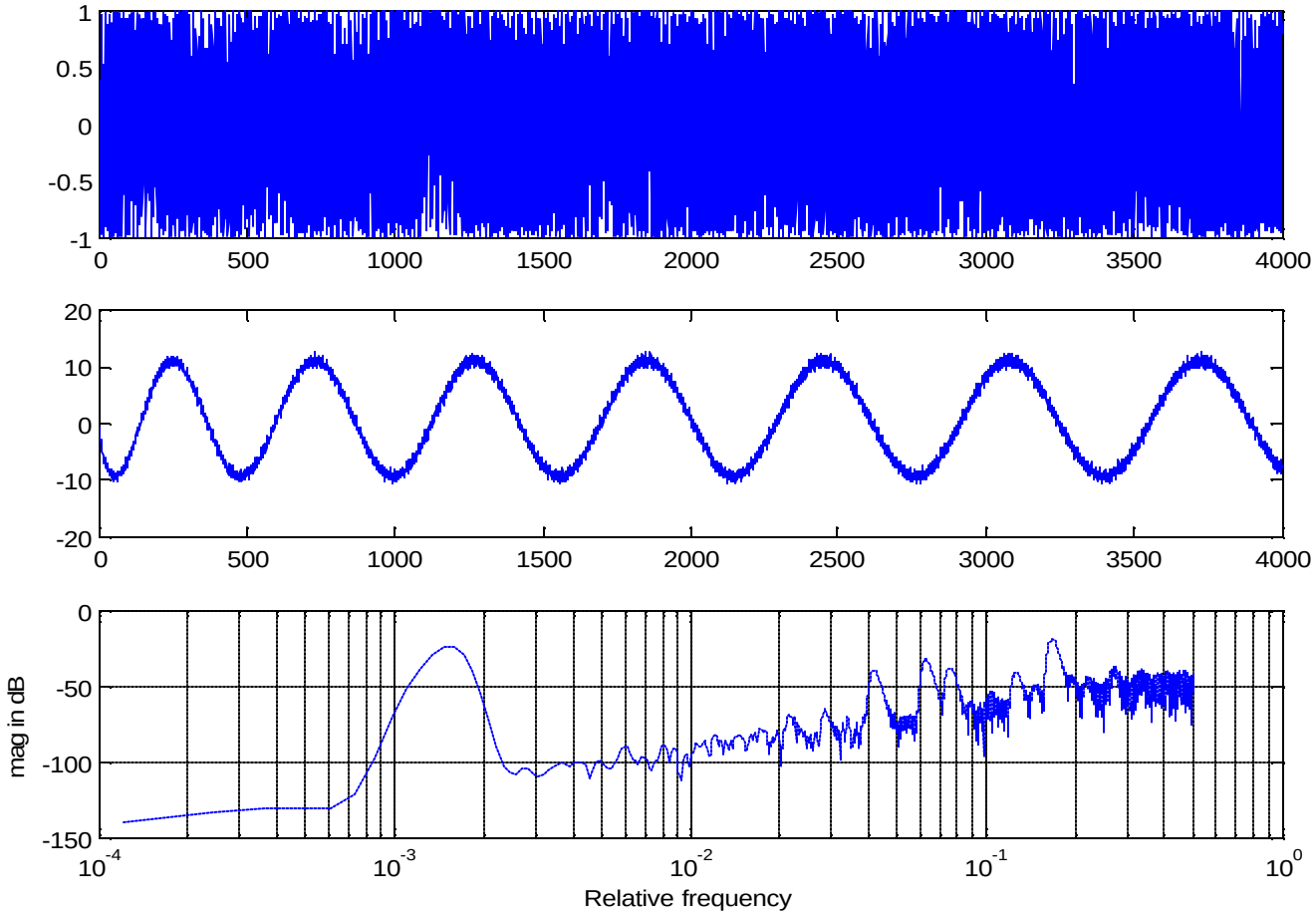


a) Values obtained by taking a vertical slice of the array of 1st 4000 waves at t=3

b) Cumulative sum (integral) of a).

c) Spectrum of a) using Kaiser window.

Slice at 3.01



a) Values obtained by taking a vertical slice of the array of first 4000 waves at t=3 +0.01,

b) Cumulative sum (integral) of a).

c) Spectrum of a) using Kaiser window.